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Transistor-Level Optimization of Three Input XOR/XNOR Gate Using CMOS Logic Design

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Abstract: Power consumption and delay are two important considerations for VLSI systems. prime motive of this project is to reduce the power and to get less delay that is nothing but the high speed for any design. So Adder is one of the fundamental blocks present in arithmetic logic unit (ALU), floating point unit. Adders are very important components in some other applications such as microprocessor and digital signal processing (DSP) architectures. Digital signal processors and Microprocessors mainly rely on highly efficient implementations of generic floating point units and arithmetic logic units. The XOR/XNOR is the basic building block in many circuits like Arithmetic circuits. With the rapid growth of portable electronic devices, it is becoming a critical challenge to design low-power, high-speed (LPHS) circuits that occupy small chip areas efficient three-input XOR/XNOR circuits as the most significant blocks of digital systems with a new systematic cell design methodology (SCDM) in hybrid-CMOS logic style. SCDM, which is an extension of CDM, plays the essential role in designing efficient circuits. At first, it is deliberately given priority to general design goals in a base structure of circuits. This simulation was carried out using TSMC018 in Tanner EDA Tool.

Keywords: XOR/XNOR, SCDM, Hybrid CMOS.

I. INTRODUCTION

With the rapid growth of portable electronic devices, it is becoming a critical challenge to design low-power, high-speed (LPHS) circuits that occupy small chip areas. Many published papers that compete in designing better circuits. Such studies mostly rely on creative design ideas but do not follow a systematic approach. As a consequence, most of them suffer from some different disadvantages.

- They are implemented with logic styles that have an incomplete voltage swing in some internal nodes, which leads to static power dissipation.
- Most of them suffer from severe output signal degradation and cannot sustain low-voltage operation.
- They predominantly have dynamic power consumption for non-balanced propagation delay inside and outside circuits, which results in glitches at the outputs.

Therefore, a well-organized design methodology can be regarded as a strong solution for the challenge. It is not try-and-error-driven, which means that it systematically and deliberately aims to the design goals. It also picks circuit components wisely and does not postpone the determination of the circuit characteristics after simulation. Cell design methodology (CDM) has been presented to design some limited functions, such as two-input XOR/XNOR and carry–inverse carry in the hybrid-CMOS style. The predominant results persuade us to improve CDM through two stages:

- Generating more complex functions and
- Rectifying some remaining flaws.

The flaws in previously published CDM include containing some manual steps in the design flow and generating a large number of designs in which the predominant ones would be determined after the completion of simulations. Complementary Metal Oxide Semiconductor (CMOS) technology is advancing for microprocessors. Supply voltage (Vdd) and transistor size continue to scale smaller sizes with lower power dissipation and faster microprocessors. The exclusive-OR (XOR) and exclusive-NOR (XNOR) functions are popular gates in microprocessors. The XOR/XNOR gates are fundamental unit circuits used in comparators, parity checkers, error detectors and correctors, multipliers, adders (ALU, AGU), etc. Many circuit implementations of XOR/XNOR gates have been proposed previously. In this project the SCDM methodology for design of XOR/XNOR gate design is implemented. Systematic Cell Design Methodology (SCDM) in designing the three-input XOR/XNORs for the first time. It systematically generates elementary basic cell (EBC) using binary decision diagram (BDD), and wisely chooses circuit components based on a specific target. Therefore, after the systematic generation, the SCDM considers circuit optimization based on our target in three steps:

- Wise selection of the basic cell;
- Wise selection of the amend mechanisms; and
- Transistor sizing.

It should be noted that BDD can be utilized for EBC generation of other three-input functions.

- Proposed System AdvantagesThe least number of transistors in critical path increases the chances of the

circuit to have better characteristics, as experimental results have shown an average savings in terms of delay, Power-Delay Product (PDP), Energy-Delay Product (EDP), respectively.

- Power-ground-free main structure leads to power reduction.

II. DESIGN AND IMPLEMENTATION

A. SCDM for Three-Input Xor/Xnor Circuits

In the first stage, a three-input XOR/XNOR as one of the most complex and all-purpose three-input basic gates in arithmetic circuits has been chosen. If the efficiency of the circuits is confirmed in such a competitive environment, it can show the strength of the methodology. In the second stage, CDM is matured as systematic CDM (SCDM) in designing the three-input XOR/XNORs for the first time. It systematically generates elementary basic cell (EBC) using binary decision diagram (BDD), and wisely chooses circuit components based on a specific target. This takes place when the mentioned features are not considered in the CDM. Therefore, after the systematic generation, the SCDM considers circuit optimization based on our target in three steps: 1) wise selection of the basic cell; 2) wise selection of the amend mechanisms; and 3) transistor sizing. It should be noted that BDD can be utilized for EBC generation of other three-input functions. We consider the power-delay product (PDP) as the design target. It stands as a fair performance metric, precisely involving portable electronic system targets.

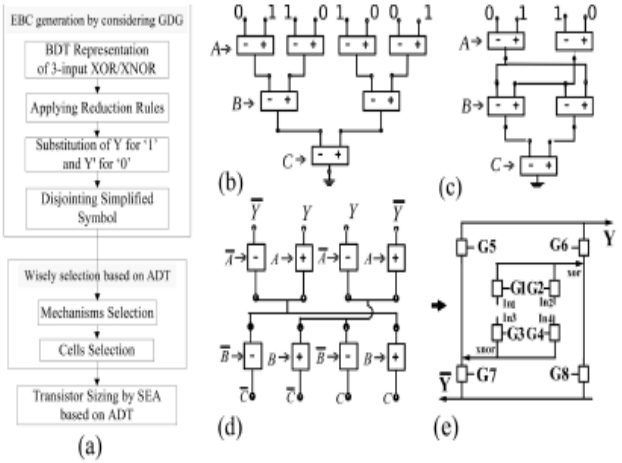

Fig.1. (a) SCDM Process for Designing Efficient Three-Input XOR/Xnors. (b) BDT Representation of Three-Input XOR/XNOR Function. (c) Applying Reduction Rules. (d) Substitution and Disjointing. (e) EBC

A. Elementary Basic Cell Systematic Generation

In order to generate the EBC of three-input XOR/XNOR circuits, four steps are taken. Initially, three-input XOR and its complement is represented by one binary decision tree (BDT) in order to share common sub circuits. The BDT is achieved by some cascaded 2 ×1 MUX blocks, which are denoted by simplified symbol controlled with input variables at each correspondent level. This construction simply implements the min-terms of the three-input XOR/XNOR function. The step is followed by applying reduction rules to simplify the BDT representation. These include elimination, merging, and coupling rules. The major task of the coupling rule, in simple terms, is to obtain all the possible equivalent trees by interchanging the order of the controls. The trees are acquired by impacting the state matrix on the corresponding control matrix where the multiply and add operators operate as follows

$$0\_\cdot \chi i = \chi$$
$$1\_\cdot \chi i = \chi$$
$$\chi 1$$
$$+\hat{} \chi 2$$
$$+\hat{} \cdot \cdot \cdot +\hat{} \chi m = \chi 1 \chi 2 \ldots \chi m = 11 \ldots 1 = I2m-1. \quad (1)$$

The result of applying the reduction rules to the tree. Afterward, as the inputs into the first level are 0's and 1's of the function's truth table, the 0 and 1 can be replaced by the *Y'* and *Y* , respectively. Finally, the simplified symbol can be divided into two distinct symbols: 1) the plus sign with the *x* input control and 2) the minus sign with the *x_* input control. The result of applying steps 3 and 4. The EBC, which is extracted from the above procedure, has been presented. This cell has eight elements, deciding two outputs. We refer to the pins of the central section (IN1–IN4 and G1–G4) as *A* or *C*, or their complements. We also assume that pins of the external section *G*5–*G*8 can also be *B* or its complement.

III. INTRODUCTION OF THE STRUCTURE OF THREE-INPUT XOR/XNOR CIRCUITS WITH THE AVERAGE PDP IN FEMTOJOULE

TABLE I

Circuits	centeral part				external part				avg
	BC	mechanisms F	B	P	BC	mechanisms F	B	P	PDP
XO1	TG				C1	Fnp	-	-	1.27
XO2	C2	Fnp	-	-	C2	Fnp	-	-	0.70
XO3	TG				C2	Fp	-	-	0.62
XO4	TG				TG				0.42
XO5	TG				C1	Fnp	-	✓	0.71
XO6	C2	Fnp	-	-	C2	Fnp	-	✓	0.57
XO7	TG				C2	Fp	-	✓	0.47
XO8	TG				C1	-	p&n	✓	0.86
XO9	C2	Fnp	-	-	C2	-	p	✓	0.65
XO10	TG				C2	-	n	✓	0.50

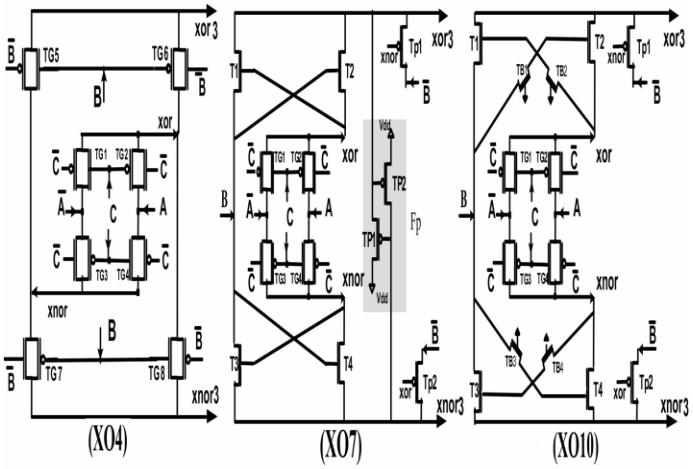

Fig.2. Three-Input XOR/XNOR Circuits, XO4, XO7, and XO10.

To control the volume of this brief, only the simulation results of the conventional and three of the best proposed circuits in terms of average PDP according to Table, XO4, XO7, and XO10, are tabulated in Table. The ascending order of delay, which is the maximum delay between all the possible transitions, as well as PDP It is apparent that among the circuits, XO4 and XO7 have the smallest delays. XO7 has slightly less delay than the XO4 at lower supply voltages. However, the trend will reverse at higher supply voltages. Hernandez1 has the second position. The circuits XO10, TF, and 18 T_NEW_FS follow the Hernandez1. In the common circumstances, the circuits utilizing FP, such as XO7 is superior to the circuits utilizing BP like XO10, which is compatible with the delay trend of mechanisms. The circuits with *C*2 like XO10 and XO7 also perform better than the circuits with *C*1. Since bootstrap technique saves the internal node voltages, the average power dissipation under different supply voltages shows that PB has less power dissipation in common situation. XO10 employing BP outperforms XO7 employing FP with regard to average power. According to the PDP trend in Fig. 2, the ability of TG to provide full-swing leads to the best circuit with optimum performance and drivability as among the circuits, XO4 has the lowest PDP. After that, circuits XO7 and XO10 have the second and third position, respectively. PDP of XO7 is less than that of XO10 for lower voltages but the trend reverses for higher voltages. Hence, from energy point of view, XO7 is a better choice. The circuits, such as XO7 using FP outperform the circuits using F. The circuits with *C*2 like XO7 and XO10 offer less PDP than the circuits with *C*1.

A. Based on Full Restored Combination Circuit Design of XOR/XNOR

In the proposed circuit we designed in the internal circuit with Complementary Transistors Logic and External with Transmission Gate as used in XOR4 Combination XOR/XNOR circuit designs are shown. The XOR/XNOR gates are given the structure names off full restored combination circuit design XOR/XNOR, complementary pass gate logic, complementary pass gate logic cross bar, swing restored gate logic, and full restored Combination circuit design XOR/XNOR with driving output.

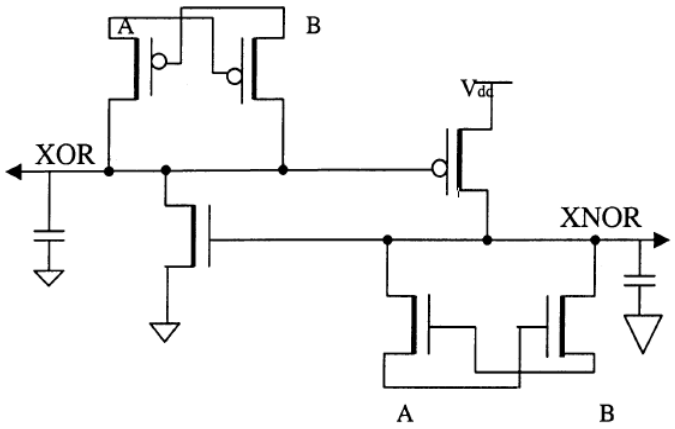

Fig.3. Full Restored Combination Circuit Design of XOR/ XNOR.

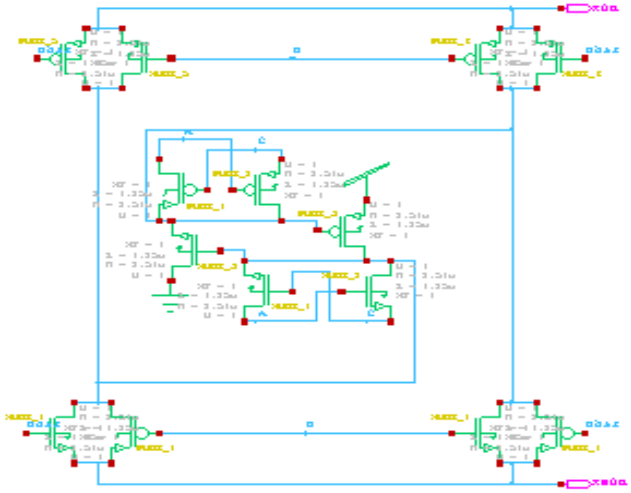

Fig.4. Three Input XOR/XNOR Design.

B. GDI based Design of Three Input XOR/XNOR

The GDI method which is first proposed by A. Morgenshtein, A. Fish, and I. A. Wagner in 2001, is based on the use of a simple cell as shown in figure.4. At first glance, the basic cell reminds the standard CMOS inverter, but there are some important differences:

- The GDI cell contains three inputs: G (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS), and N (input to the source/drain of nMOS).
- Bulks of both nMOS and pMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter. It must be remarked that not all of the functions are possible in standard p - well CMOS process but can be successfully implemented in twin - well CMOS or silicon on insulator (SOI) technologies. 2-Input XOR/XNOR gate design:

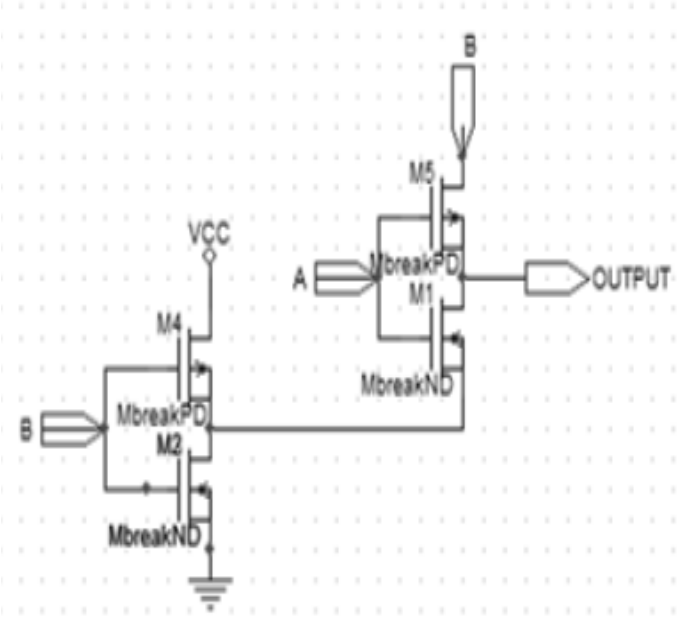

Fig.5. 2-Input XOR/XNOR Design

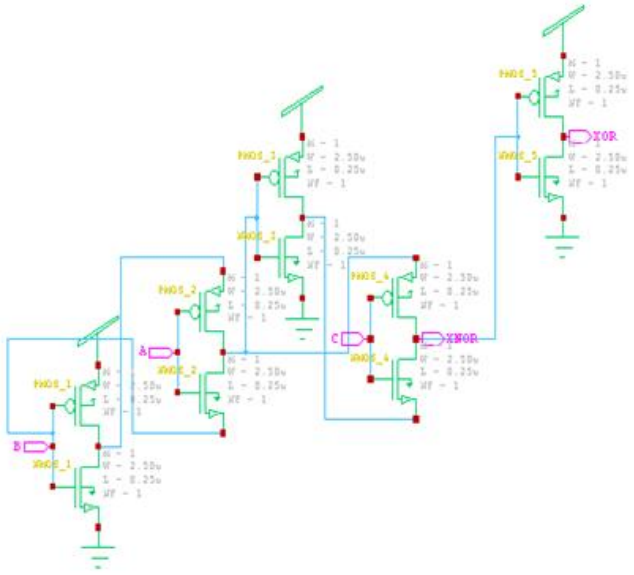

Fig.6. Three Input XOR/XNOR Design

IV. RESULT ANALYSIS

A. Existing System Circuits Results

The Following figures are schematic implementations and resultant wave forms of the existing system circuits (XO4, XO7, XO10).

B. XO4 Circuit

The schematic of the XO4 circuit was implemented in S-Edit of Tanner EDA tool. This circuit consist of two parts one is central part and another one is external part. Central part consist of four transmission gates which is connected in such a way that it gives the XOR/XNOR output of two inputs. And the external circuit consist of four transmission gates. This part takes the output of central part output as one input and the other one is direct input. The total output of the circuit can collect at external part which is three input XOR/XNOR output.

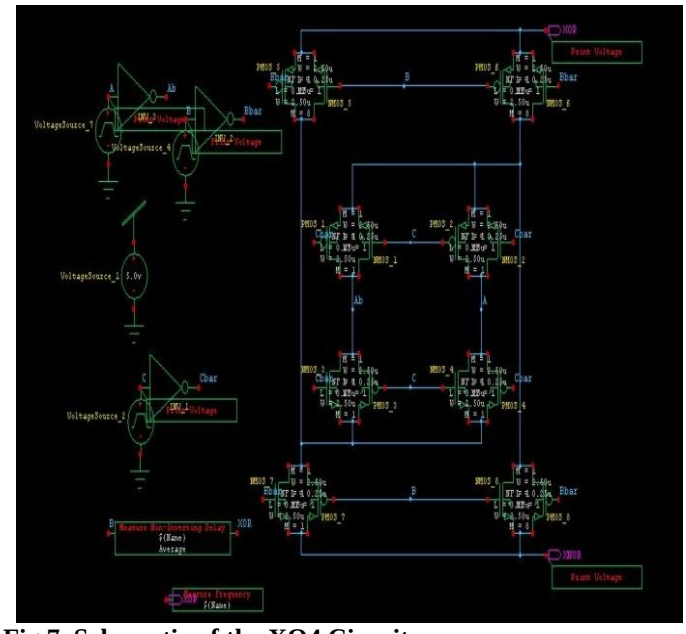

Fig.7. Schematic of the XO4 Circuit

As XO4 was designed using transmission gate technology for both external and internal part. It doesn't show any voltage degradation in their output. The below figure shows the XO4 simulation waveform with V(A), V(B), V(C) as inputs generates V(XOR) and V(XNOR) as outputs.

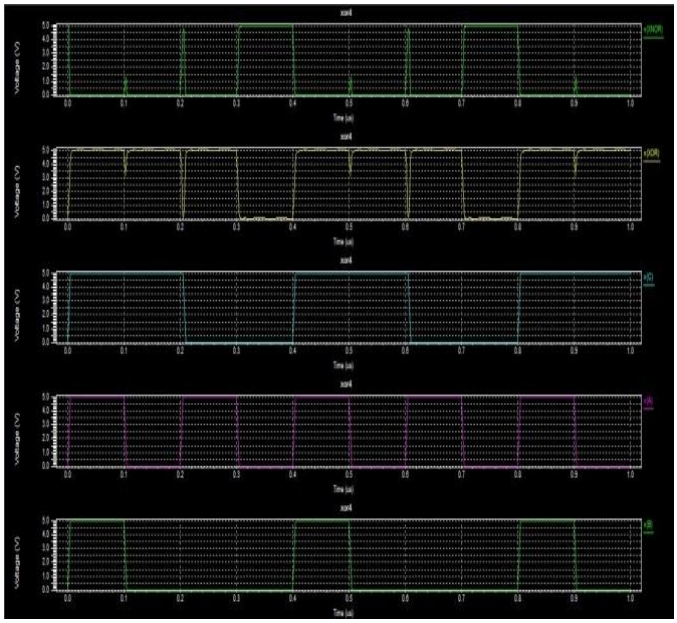

Fig.8. Resultant Waveforms of XO4 Circuit

C. XO7 Circuit

The schematic of the XO7 circuit was implemented in S-Edit of Tanner EDA Tool. This circuit is similar to the XO4 but the difference in external part i.e., instead of transmission gates here we are used PMOS and NMOS transistors. As same in XO4 we can collect the output at external part which is three input XOR/XNOR output.

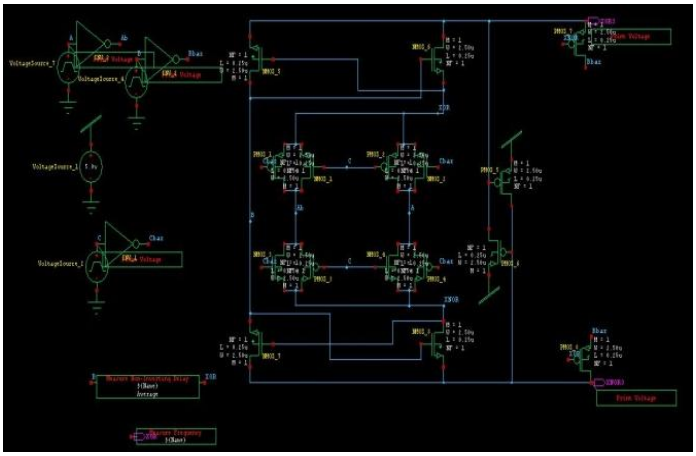

Fig.9. Schematic of XO7 Circuit.

As XO7 was designed using transmission gate technology for internal part and Pull-up, pull-down network technology for external part. It shows some voltage degradation in their output. The below figure shows the XO7 simulation waveform with V(A), V(B), V(C) as inputs generates V(XOR) and V(XNOR) as outputs.

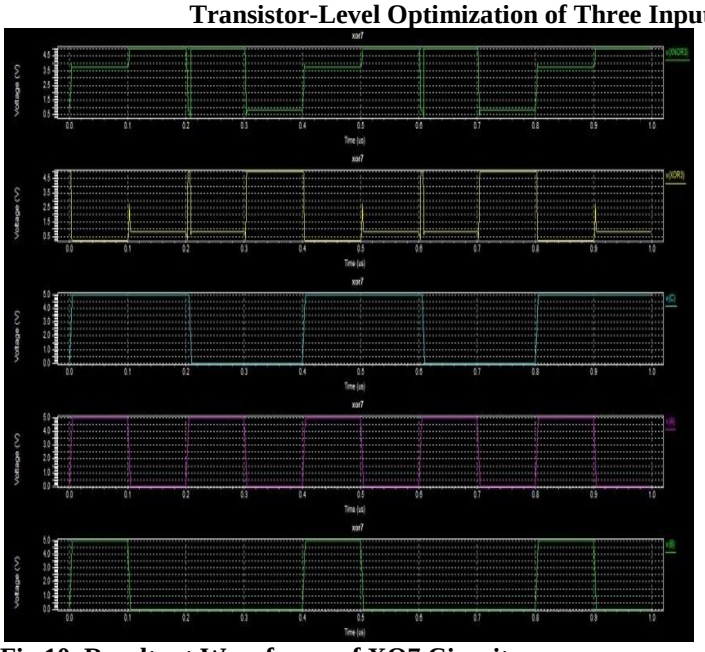

Fig.10. Resultant Waveforms of XO7 Circuit.

D. XO10 Circuit

The schematic of XO10 was implemented in S-Edit of Tanner EDA tool. This circuit is also similar to the XO4 circuit. Here also the difference is same as XO7 i.e., the mechanism of the external part. Here we can collect the output at external part.

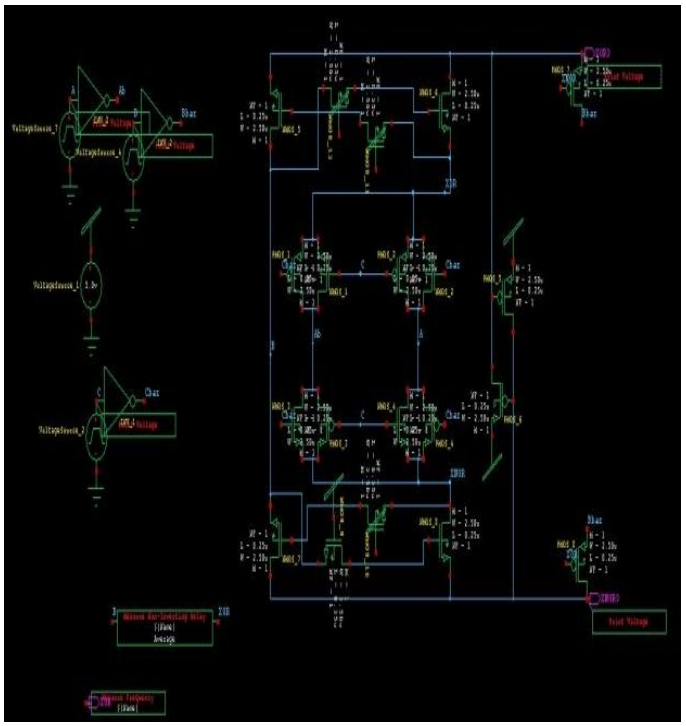

Fig.11. Schematic of the XO10 Circuit.

As XO10 was designed using transmission gate technology for internal part and Pull-up, pull-down network technology for external part. It shows some voltage degradation in their output. The below figure shows the XO10 simulation waveform with V(A), V(B), V(C) as inputs generates V(XOR) and V(XNOR) as outputs.

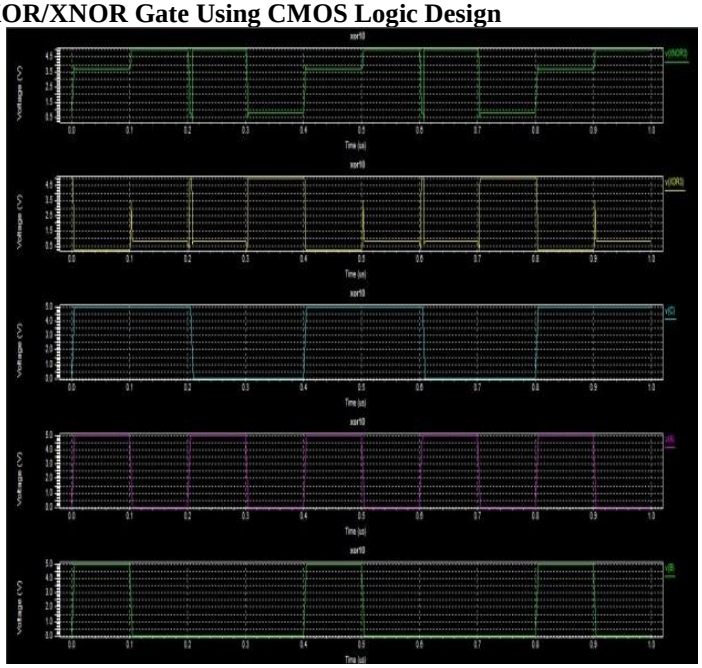

Fig.12. Resultant Waveforms of XO10 Circuit

V. PROPOSED SYSTEM CIRCUITS RESULTS

A. Modified XO4 with Full Restored Combinational Circuit

The schematic of First Proposed circuit was designed and implemented in S-Edit of Tanner EDA tool. This circuit is the extension of existing system circuits. This circuit consist of central part and external part. Central part which is designed with Fully Restored Combinational circuit which gives the output of two inputs. External part consist of four transmission gates. This external part is same as the external part of XO4 circuit. This circuit gives the output of three input XOR/XNOR.

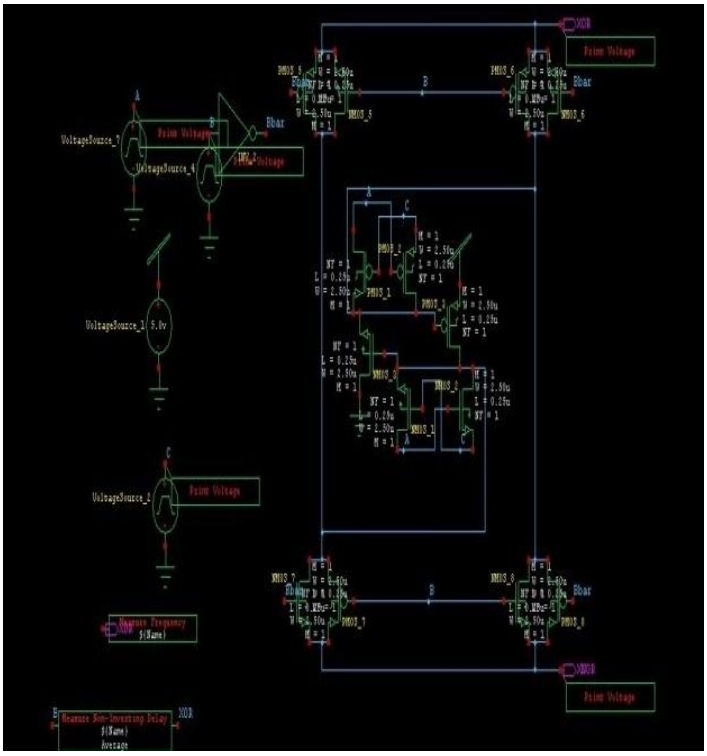

Fig.13. Schematic of Modified XO4 Circuit.

As Modified XO4 was designed using transmission gate technology for external and Pull-up, pull-down network technology for internal part. It doesn't show any voltage degradation in their output. The below figure shows the Modified XO4 simulation waveform with V(A), V(B), V(C) as inputs generates V(XOR) and V(XNOR) as outputs.

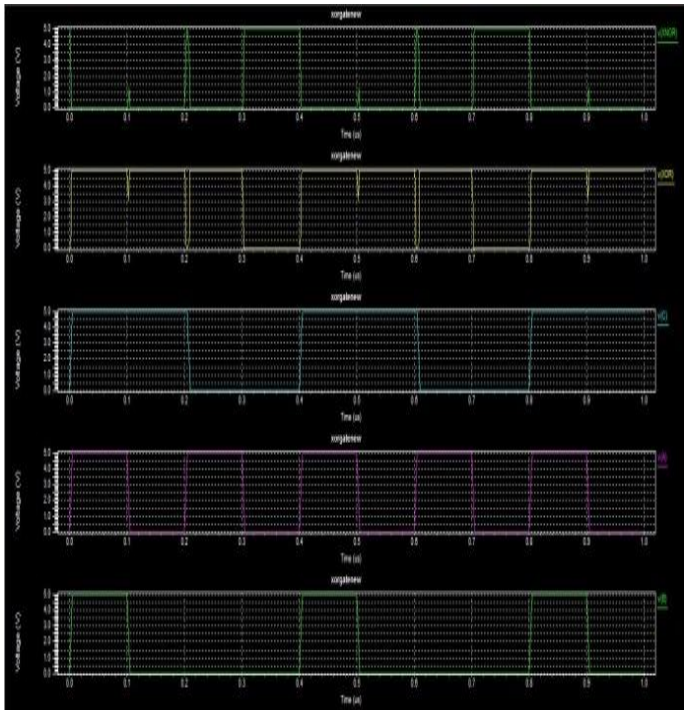

Fig.14. Resultant Waveforms of Modified XO4 Circuit

B. GDI Based XOR-XNOR Circuit

The schematic of Second Proposed circuit was designed and implemented in S-Edit of Tanner EDA tool. This circuit is the extension of existing system circuits. This circuit was GDI based Design which gives the output as three input XOR/XNOR output.

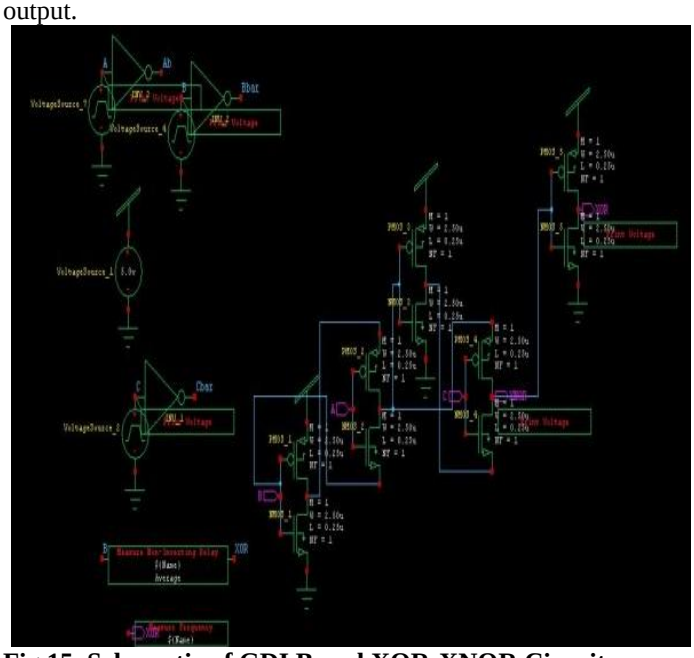

Fig.15. Schematic of GDI Based XOR-XNOR Circuit.

GDI based XOR-XNOR circuit was designed. It shows some voltage degradation in their output. The below figure shows the GDI based XOR-XNOR circuit simulation waveform with V(A), V(B), V(C) as inputs generates V(XOR) and V(XNOR) as outputs.

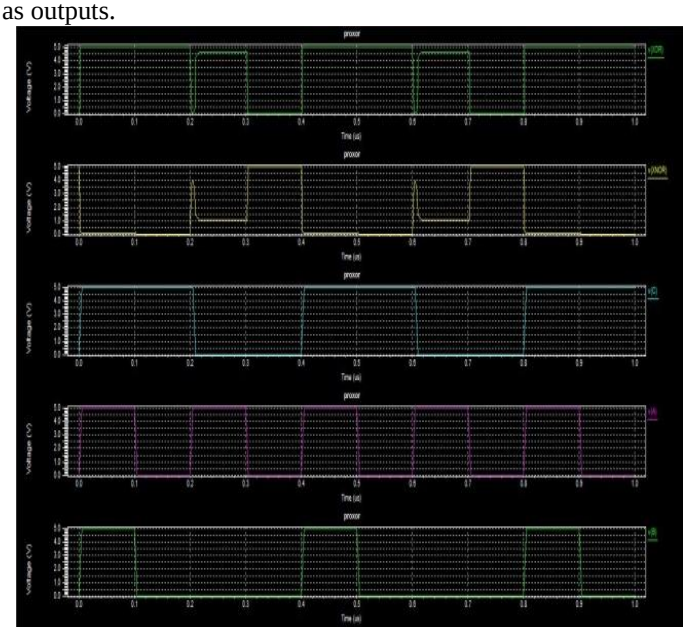

Fig.16. Resultant Waveforms of GDI based XOR-XNOR Circuit.

The below tables shows the values of the some parameters of each and every circuit:

TABLE II. Parameter Values of the Circuits

	Avg Power	Avg Delay	Avg PDP	Avg EDP	Area
XO4	0.0047	5.08E-08	2.39558E-10	1.21E-17	13.7
XO7	0.00978	1E-07	9.81E-10	9.81E-16	13.7
XO10	0.00979	1E-07	9.7448E-10	9.74E-17	16.25
Modified XO4	2.78E-04	4.99E-08	1.38722E-11	6.92E-19	10
GDI based XOR-XNOR	1.17E-03	4.89E-08	5.62E-11	2.74E-18	10

TABLE III. Parameter Values of the Circuits

	Tr#	Density	Max freq(Hz)	Static Power(Watts)	Total o/p noise vol(sq v/Hz)
XO4	22	1.6	4.88E+06	1.03E-08	15.53215
XO7	22	1.6	9.53E+06	7.95E-03	10.46534
XO10	26	1.6	9.53E+06	8.13E-03	10.21752
Modified XO4	16	1.6	4.85E+06	1.57E-08	10.83391
GDI based XOR-XNOR	16	1.6	4.81E+06	1.96E-04	8042934

The below graph represents the Avg Power consumptions of the different Circuits:

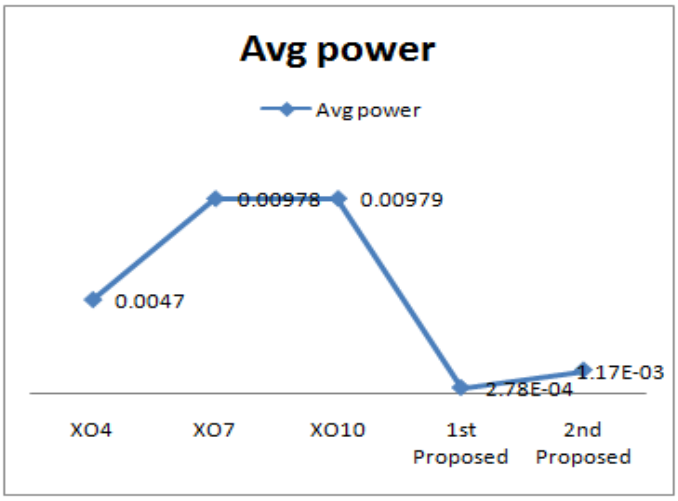

Fig.17.Avg Power of Existing and Proposed Circuits.

The below graph represents the Avg Delay of the different Circuits:

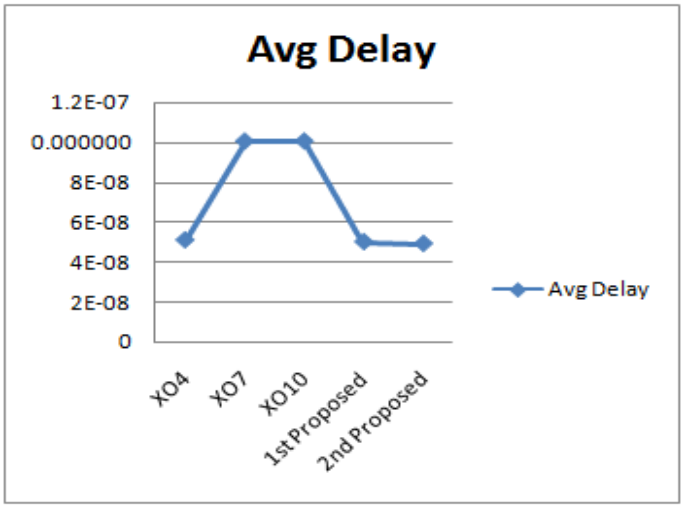

Fig.18. Avg Delay of Existing and Proposed Circuits.

The below graph represents the Avg PDP of the different Circuits:

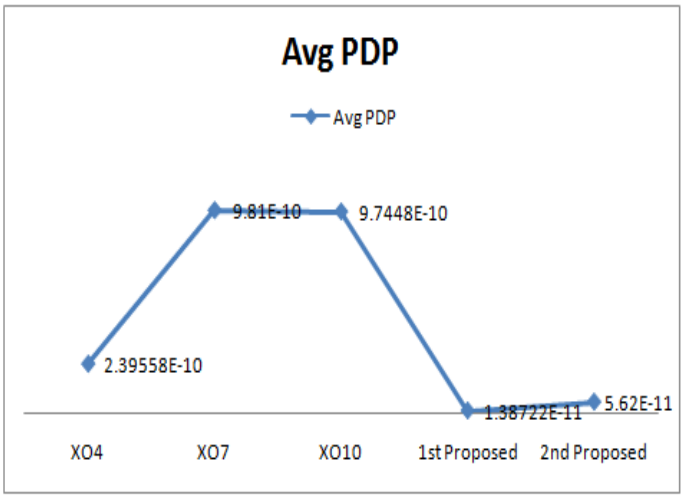

Fig.19. Avg PDP of Existing and Proposed Circuits.

The below graph represents the Avg EDP of the different Circuits:

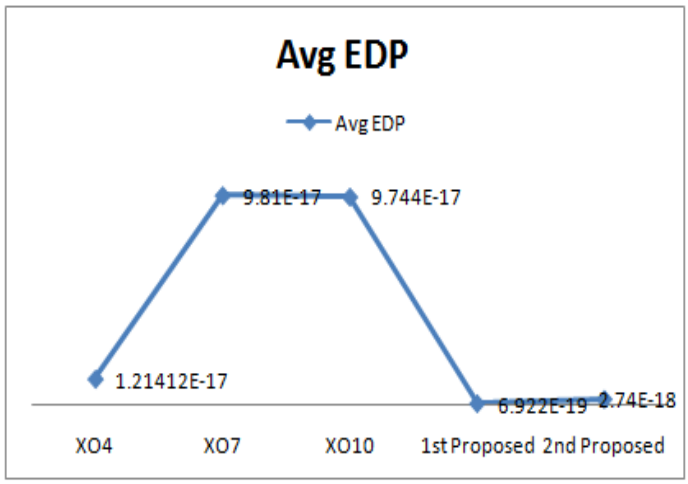

Fig.20. Avg EDP of Existing and Proposed Circuits.

The below graph represents the Area of the different Circuits: Area in terms of no. of transistors used by the circuit.

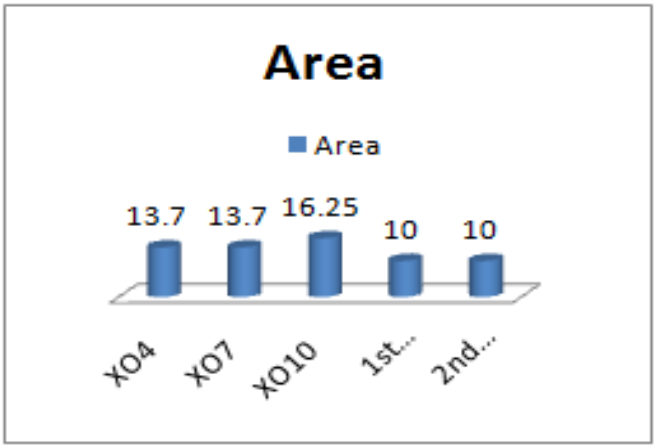

Fig.21.Area of Existing and Proposed Circuits.

VI. CONCLUSION

In this project two novel design methodologies of low voltage XOR-XNOR circuits are tested. The performance of the proposed circuits can operate at low-voltages, and have good output levels. The proposed circuits tested to have noise-immunity, higher energy-efficiency and faster operation. In the end, new high performance three-input XOR-XNOR circuits with less PDP and occupied area are designed.

VII. REFERENCES

[1]C.-K. Tung, S.-H. Shieh, and C.-H. Cheng, "Low-power high-speed full adder for portable electronic applications," Electron. Lett., vol. 49, no. 17, pp. 1063–1064, Aug. 2013.

[2]M. Aguirre-Hernandez and M. Linares-Aranda, "CMOS full-adders for energy-efficient arithmetic applications," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 4, pp. 718–721, Apr. 2011.

[3]M. H. Moaiyeri, R. F. Mirzaee, K. Navi, T. Nikoubin, and O. Kavehei, "Novel direct designs for 3-input XOR function for

low-power and highspeed applications," Int. J. Electron., vol. 97, no. 6, pp. 647–662, 2010.
[4]S. Goel, M. A. Elgamel, M. A. Bayoumi, and Y. Hanafy, "Design methodologies for high performance noise-tolerant XOR-XNOR circuits," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 53, no. 4, pp. 867–878, Apr. 2006.
[5]T. Nikoubin, M. Grailoo, and S. H. Mozafari, "Cell design methodology based on transmission gate for low-power high-speed balanced XOR-XNOR circuits in hybrid-CMOS logic style," J. Low Power Electron., vol. 6, no. 4, pp. 503–512, 2010.
[6]T. Nikoubin, A. Baniasadi, F. Eslami, and K. Navi, "A new cell design methodology for balanced XOR-XNOR circuits for hybrid- CMOS logic," J. Low Power Electron., vol. 5, no. 4, pp. 474–483, 2009.
[7]T. Nikoubin, M. Grailoo, and C. Li, "Cell design methodology (CDM) for balanced Carry Inverse Carry circuits in hybrid-CMOS logic style," Int. J. Electron., vol. 101, no. 10, pp. 1357–1374, 2014.
[8]A. Eshra and A. El-Sayed, "An odd parity checker prototype using DNAzyme finite state machine," IEEE/ACM Trans. Comput. Biol. Bioinf., vol. 11, no. 2, pp. 316–324, Mar./Apr. 2014.
[9]R. Roy, D. Bhattacharya, and V. Boppana, "Transistor-level optimization of digital designs with flex cells," Computer, vol. 38, no. 2, pp. 53–61, Feb. 2005.
[10]A. M. Shams, T. K. Darwish, and M. A. Bayoumi, "Performance analysis of low-power 1-bit CMOS full adder cells," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 10, no. 1, pp. 20–29, Feb. 2002.
[11]J.-F. Lin, Y.-T. Hwang, M.-H. Sheu, and C.-C. Ho, "A novel high-speed and energy efficient 10-transistor full adder design," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 54, no. 5, pp. 1050–1059, May 2007.