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Optimization of Power in Flip-Flop Group using Clock Gating and Power Gating with Variable Body-Bias Technique

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Abstract: Energy dissipation is a very critical parameter that has to be taken into account during the design of Very Large Scale Integration (VLSI) circuits. With the rapid progress in semiconductor technology, chip density and operation frequency have increased, making the power consumption in battery-operated portable devices a major concern. Integrated Circuit (IC) power dissipation consists of different components depending on the circuit operating mode. First, the switching or dynamic power component dominates during the active mode of operation. Second, there are two primary leakage sources, the active component and the standby leakage component. Clock gating and power gating proves to be very effective solutions for reducing dynamic and active leakage power respectively. The two techniques are coupled in such a way that the clock gating information is used to drive the control signal of power-gating circuitry. First, a technique named Optimized Bus-Specific-Clock-Gating (OBSC) is introduced which reduces the problem of gated flip-flop selection by appropriate selection of subset of flip-flops. Then another technique named Run Time Power Gating (RTPG) is proposed for power gating the combinational logics performing redundant operations. The proposed shift registers are designed up to the layout level with 1V Power supply in 0.18um technology and simulated using Tanner Tools.

Keywords: Clock Gating, Power Dissipation, Power Gating, OBSC, RTPG.

I. INTRODUCTION

Today's consumer demands more functionality, energy efficient device and optimized power devices as time goes, so in order to optimize power of a device the simplest control technique is to shut off the clock of the sequential block of the device when there is no function required from that section for some duration With the smaller geometries in Deep Sub-Micron (DSM) technology, the number of gates that need to be integrated on a single chip, power density, and total power are increasing rapidly. The scaling of process technologies to nanometer regime has resulted in a rapid increase in leakage power dissipation [1]. Integrated Circuit (IC) power dissipation consists of different components depending on the circuit operating mode. First, the switching or dynamic power component dominates during the active mode of operation. Second, there are two primary leakage sources, the active component and the standby leakage component. The standby leakage may be made significantly smaller than the active leakage by changing the body bias conditions or by Power Gating. Clock gating and power gating proves to be terribly effective solutions for reducing dynamic and static leak power respectively[2]. As active leakage power becomes more and more important it also requires care. In order to distinguish it from the traditional PG, which is used to reduce the standby leakage, the PG to minimize active leakage power in the operation mode is referred to as run time power gating (RTPG), CG is a technique used to gate the unnecessary clock toggles of a register. During the clock gated period, there are some components that are performing redundant operations, and RTPG will put these components into sleep[3].

II. CLOCK GATING AND POWER GATING

A. Clock Gating

Clock gating is one of the well known and effective power optimization technique in VLSI circuits. Its aim is to suppress the propagation of transitions within the circuit under some conditions satisfied by clock gating circuitry. The main source of power dissipation in circuits are due to charging and discharging of the capacitors. So if the transitions, switching activities at the nodes decreases and the power dissipation reduces[4].

B. Proposed OBSC Circuit

Optimized Bus Specific Clock Gating is very effective technique to maximize dynamic power reduction as shown in fig1. It chooses only a subset of flip-flops (FF) to be gated selectively, and the problem of gated FF selection is reduced from exponential complexity into linear. It works by comparing the inputs and outputs and gates the clock when they are equal[5][4]. Suppose there are N FFs in the non CG circuit, each FF can be chosen as gated or non gated. So there will be 2N possible CG solutions. One of the contributions of this brief is that this exponential complexity problem is reduced into linear by using the signal activity information. All the FFs are chosen to be gated initially, then the problem becomes how to determine which FFs should be excluded from gating. This is because that maximum output data toggle rate indicates that

minimum clock toggles will be gated, thus power will reduce least or even increase if the FF is gated. More formally, the FF with the maximum output toggle rate is excluded from gating first, then the FF with the second largest output toggle rate is excluded and so on until all the FFs are excluded. Apparently, during the process of exclusion, there will be N+1 possible CG solutions which is linear complexity[4][2][1][5].

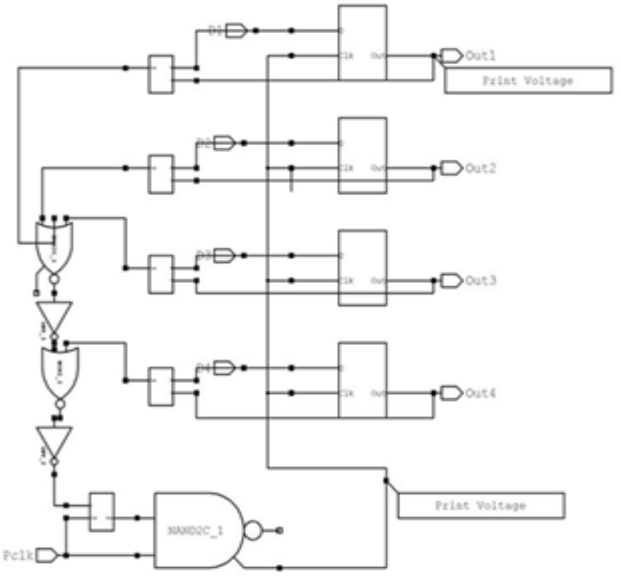

Fig.1. Proposed OBSC Circuit.

C. Power Gating

As the scaling of MOS Transistor proceeds, leakage power of VLSI chips increases dramatically. Leakage power has been a major concern in portable devices because it wastes energy at standby mode and leads to shortening the battery life. One of the effective techniques to reduce stand by leakage current is power gating in which a power switch is inserted between logic circuits and the ground [5]. In the standby mode, the power switch is turned off to electrically disconnect the logic circuits from the ground, resulting in cutting off the leakage. Power gating is a technique used in integrated circuit design to reduce power consumption, by shutting off the current to blocks of the circuit that are not in use. In addition to reducing stand-by or leakage power, power gating has the benefit of enabling Iddq testing[1].

D. Proposed RTPG Circuit

Power gating is the most effective available technique to reduce stand by leakage, with benefits that are magnified by the increasing fraction of overall IC lifetime that modules spend in stand-by mode. With technology scaling, active-mode leakage becomes an increasingly significant portion of total dynamic power. The Proposed Run-Time Power Gating (RTPG) to extend the application of power gating to active-mode leakage reduction[5]. Fig 2 shows the basic structure that we use for fine-grained RTPG. We fully exploit the enable signals of gated clock design to control both power switches provided to the combinational logic gates and holders. The holder is composed of low leakage transistors (e.g. high-V^{th} and thicker gate oxide) and inserted between power-gated and non-power-gated circuits. When the enable signal is 0, the power switch is turned off and active leakage current is cut off at the power-gated logic circuits. The holders keep the input voltage of the non-power-gated circuits to avoid signal floating. When the enable signal is 1, the power switch is turned on and updated data are loaded into the F/F.

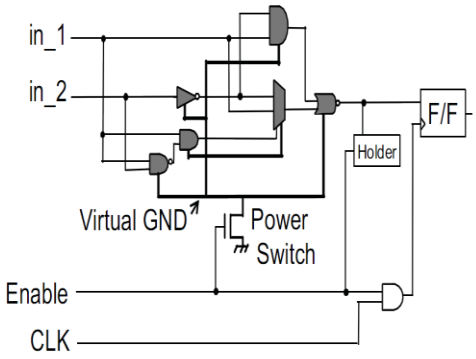

Fig.2. Basic structure for Run time power gating.

III. INTEGRATION OF OBSC AND RTPG

In order to achieve integration of CG and RTPG, apply OBSC technique to the design, then a subset of FFs is clock gated. During the clock gated period, the outputs of the gated FFs are stable. Consequently, those combinational logics whose inputs only depend on gated FF outputs will be inactive and can be power gated. For each output of the power gated cell, whether a connection to primary output presence has to be checked.

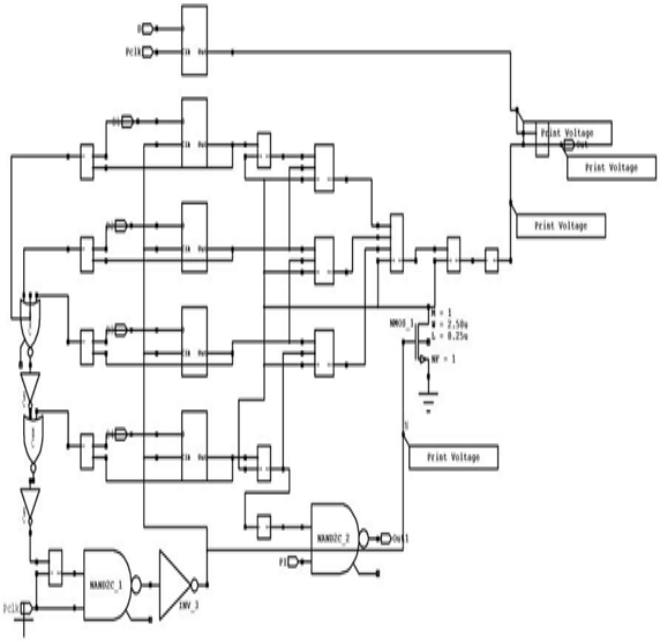

Fig.3. Integration of OBSC and RTPG.

Holder logic should be added in order to avoid signal floating. Suppose that four out of five FFs are clock gated. The circled cells are completely dependent on the stable gated FF outputs, so they are not active and can be power gated into sleep. However, one input of the XOR gate i is the output of

ungated FF A, and one input of the AND gate h is the primary input. Since both the ungated FF output and PI may not be stable during the clock gated period, the XOR gate i and the AND h may be active. So they should not be power gated. In order to avoid floating signal, a holder should be placed at the output of each power gated cell if that output connects to non power gated cells or primary outputs (POs)[5]. If RTPG has to be applied, a footer (high-Vth CMOS transistor) between the actual ground and virtual ground of the power gated cells should be added. After the integration of CG and RTPG, the low power design should look like Fig 3. The enable signal generated from OBSC is used as the sleep signal for the PG. The cells that are totally dependent on gated FF outputs are power gated. Holders are placed between the power gated cells and the non power gated cells so that the non power gated cells can function properly.

IV. VARIABLE BODY BIASING TECHNIQUE

This is another new leakage reduction technique, which we call the ‘’Variable body biasing’’ technique.

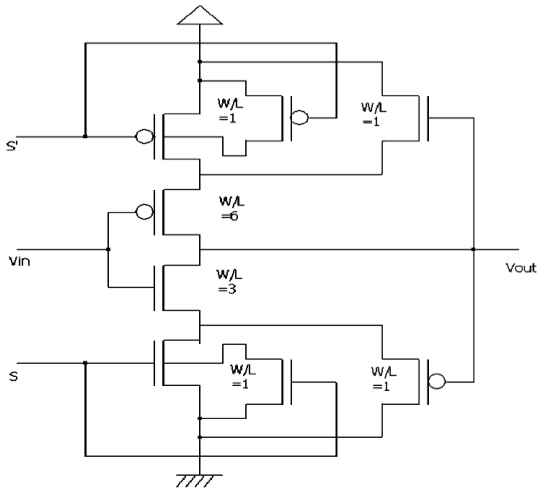

Fig.4. Structure of variable body biasing technique with sleep method.

This technique in fig 4, uses two parallel connected sleep transistors in V_{dd} and two parallel connected sleep transistors in GND. The source of one of the PMOS sleep transistor is connected to the body of other PMOS sleep transistor for having so called body biasing effect. Similarly the source of one of the NMOS sleep transistor is connected to the body of other NMOS sleep transistor for having the same effect as for PMOS sleep transistors. So, leakage reduction in this technique occurs in two ways. Firstly, the sleep transistor effect and secondly, the variable body biasing effect. It is well known that PMOS transistors are not efficient at passing GND; similarly, it is well known that NMOS transistors are not efficient at passing V_{dd}. But this variable body biasing technique uses PMOS transistor in GND and NMOS transistor in V_{dd}, both are in paralleled to the sleep transistors, for maintaining exact logic state during sleep mode. This technique uses aspect ratio W/L=3 for NMOS transistor and W/L=6 for PMOS transistor in the main inverter portion. For the sleep transistors this technique uses aspect ratio W/L=1 for both the NMOS and PMOS transistors. The extra two transistors of the design for maintaining the logic state during sleep mode also use aspect ratio W/L=1.Due to the minimum aspect ratio the sub-threshold current reduces[7].

V. INTEGRATION OF OBSC AND RTPG WITH VARIABLE BODY-BIAS TECHNIQUE

Variable-threshold circuits dynamically control the threshold voltage of transistors through substrate biasing and hence overcome shortcoming associated with multi-threshold design. When a variable-threshold circuit is in standby, the substrate of NMOS transistors is negatively biased, and their threshold increases because of the body-bias effect Figs.5 and 6. Similarly the substrate of PMOS transistors is biased by positive body bias to increase their V_t in stand-by. Variable-threshold circuits can, in principle, solve the static leakage problem, but they require control circuits that modulate substrate voltage in stand-by.

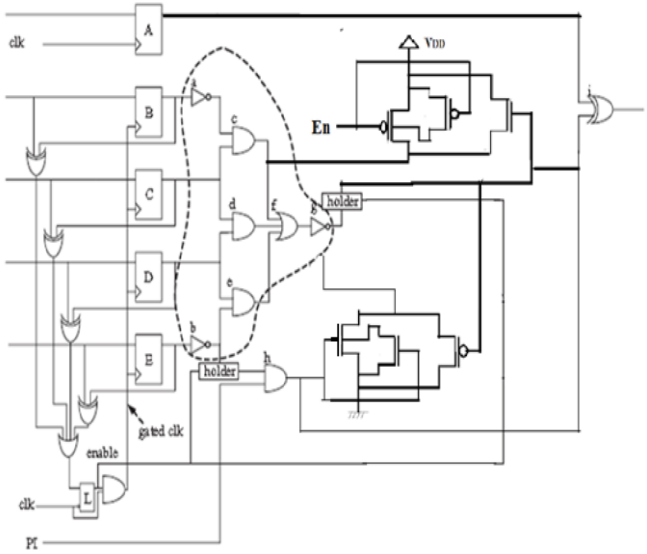

Fig.5. Integration of OBSC and RTPG with Variable Body-bias Technique.

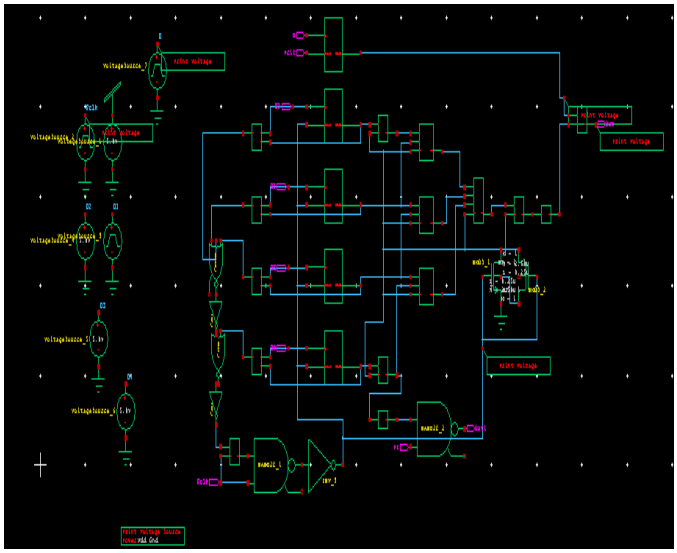

Fig.6. Schematic of OBSC with Run Time Power Gating method using Variable Body Biasing technique only to ground of chain of 5 Flip-flops.

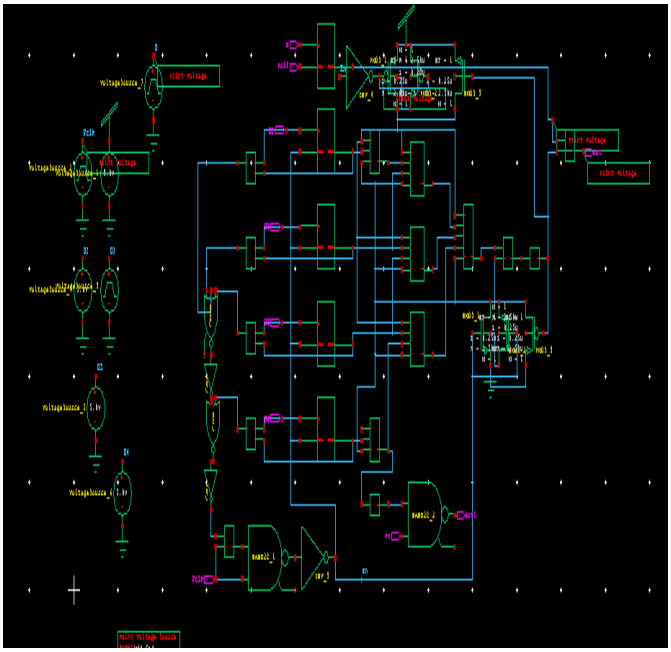

Fig.7. Schematic of OBSC with Run Time Power Gating method using Variable Body Biasing technique to power supply and ground of chain of 5 Flip-flops.

IV. RESULTS

The Integration of OBSC and RTPG with Variable Body-bias Technique method produces the following waveforms Figs.8 and 9 in the tanner tool after the simulation of the schematic circuit as shown in fig. 7.

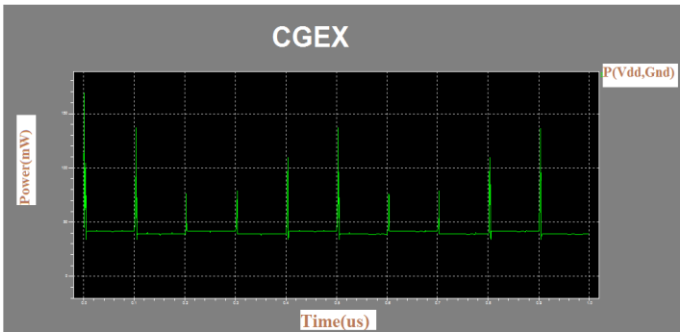

Fig.8. Graph plotted across power and time of Integrated OBSC and RTPG method using variable body biasing technique only to power supply chain of 5 Flip-flops circuit.

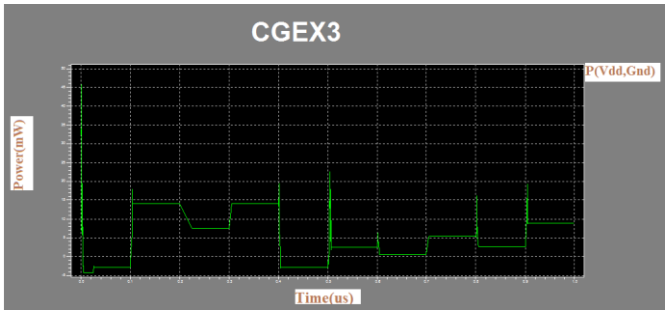

Fig.9. Graph plotted across power and time of Integrated OBSC and RTPG method using variable body biasing technique to power supply and ground of chain of 5 Flip-flops circuit.

V. PERFORMANCE ANALYSIS

Table I shows the summary of the performance on the basis of power analysis:

TABLE I: Comparison between the Power Dissipation of Circuits

Type of circuit	Power consumed
CG With RTPG	4.113243 e^{-002} W
(CGEX) CG and RTPG using Variable Body Biasing technique only to ground	4.112418 e^{-002} W
(CGEX3) CG and RTPG using Variable Body Biasing technique both to ground and power supply	5.995837 e^{-003} W

VI. CONCLUSION

In this Paper, a fine-grained CG and RTPG integration is achieved in sequential circuits. First, an activity driven fine-grained OBSC technique is evaluated that selects only a subset of FFs to gate. Moreover, the clock enable signal generated in the OBSC circuit can be used as the sleep signal in RTPG. Following this, Sequential circuits that implements both OBSC and RTPG is considered and their performances are evaluated with sleep and variable body bias technique using Tanner Tools.

Future Scope: For Integration of clock gating we must check about the delay produced the clock gating network so in future we can design which can reduce the delay produced by the clock gating circuitry.

VII. REFERENCES

[1] 1B.Blessy Dedeepya, 2Dr.G.A.E.Satish Kumar "Clock Gating and Run Time Power Gating Integration by Using Dual Stacking Technique"1P.G Student, Stanley Stephen College of Engg & Tech, Panchalingala,Kurnool. 2Vice Principal, Stanley Stephen College of Engg & Tech, Panchalingala,Kurnool.

[2] S.Sujitha, K.Radha "Design of Low Power Flip-Flop Using Clock Gating and Power Gating" PG Scholar1, Assistant professor2 Department of ECE,K.C.G College of Technology, Chennai, India.

[3] G.Lourds Sheeba, Mrs. T.C.Sabareeswari "A High Performnce Vriable Body Biasing Design with Low Power Clocking System Using MTCMOS" Department of VLSI design Madha Engineering College Chennai, India.

[4] Himanshu Chaudhary, Nitish Goyal, Nagendra Sah "Dynamic Power Reduction Using Clock Gating: A Review", PEC University of Technology, Chandigarh, UT, India.

[5] Power Efficient Design of Sequential Circuits using OBSC and RTPG Integration Rampriya.R1, Marutharaj.T2 [1]PG Scholar/ M.E VLSI Design, TKSCT, Theni, India [2]Assistant Professor, Department of ECE, TKCST, Theni, India.

[6] Kimiyoshi Usami and Naoaki Ohkubo "A Design Approach for Fine-grained Run-Time Power Gating using Locally Extracted Sleep Signals", Shibaura Institute of Technology 3-7-5 Toyosu, Kohtoh-ku, Tokyo 135-8548, Japan.

[7] Arpit Chourgade1, Sachin Bandewar2, " To Reduces the Static and Dynamic Power Dissipation through Variable Body Biasing Technique" 1Student, 2Asst. Prof. & HOD, RKDF University

[8] Jagrit Kathuria, M.Ayoubkhan, Arti Noor "A Review of Clock Gating Techniques". Center for Development of advanced computing, NOIDA India.