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An Efficient Level Converter Model for Power Optimization

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Abstract: Now a day's in all electronic devices power dissipation is the major factor this will have an impact on performance and also propagation delay of the device. This power consumption has a quadratic relation with voltage of supply. For that reason we have more power reduction techniques but each has its own constraints. Among those multi supply voltage, multi threshold logic, clock gating and dual voltage system are widely used, but most prominent model is dual voltage system (vddl, vddh). A combination of two voltage signals and a level converter which leads a very low power operated design but the major challenges by using level converters are a small amount of delay and a small amount of power. To overcome those we proposed combination of dual vth and feedback system i.e., Multi threshold feedback pass transistor level converter (MTFP). This prominently reduces delay and power consumption. For simulation Tanner EDA V.15.0 and for average power and delay calculations on H-spice 2007 by using 32nm PTM model technology.

Keywords*:* Propagation Delay, Multisupply Voltage, Multi Treshold Logic, Clockgating, Dual Voltage System, Level Converter, Feed Back System, Pass Transistor Logic.

I. INTRODUCTION

Day by day electronic gadgets like mobile phones, laptops, ipods, tablets are having very high demand but we need more time to charge battery cause of lack of power dissipation occurs in the circuits. for that reason we want to optimize this power dissipation. Generally this power dissipation is proportional to vdd2 depending on quadratic relation. If we want to reduce the power dissipation has to reduce supply voltage[1]. Shrinking supply voltage i.e., vdd, which leads to increase the performance of system. By using different approaches like multi supply voltage, multi threshold logic, clock gating and dual voltage are proposed for shrinking the supply voltage. Multi supply voltage is a technique applies to the circuits as a high voltage supply to the critical path of the circuit and low voltage supply to the non critical path of the circuit. But we have a drawback of direct assignment of the vddl and vddh. Another supply voltage shrinking method is multi threshold logic, i.e., we assign high vth to transistors for reducing power dissipation[2] and low vth to transistors to reducing delay. To combining various domains in multi supply voltage design we are using level converters. A dual voltage design requires level converters when a low voltage gate feeds a high gate voltage means conversion of vddl to vddh. And another process is a high voltage gate feeds a low gate voltage means conversion of vddh to vddl. Level converter application in dual supply voltage circuit is one of the most efficient power consumption. By finding the critical and non critical paths of the circuit[3] we use clustered voltage scaling algorithm.

II. PREVIOUS APPROACHES

Previously we have different approaches to reduce power consumption. But among those, level converters are effectively reduces power consumption. We have a basic low voltage and high voltage assignment by using Clustered Voltage Scaling (CVS) process of critical path and path density of the circuit. The main challenge in this process is, to interfacing low voltage blocks to high voltage blocks it persists overheads delay of the system and also static current flow[4]. Shown in Fig.1.

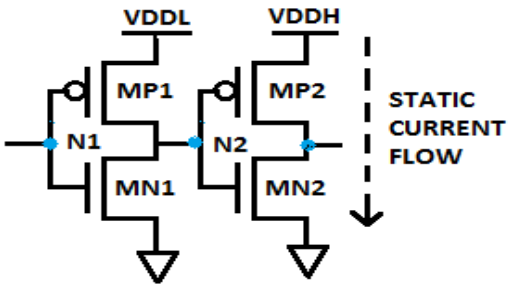

Fig.1. Dual supply voltage process[10].

But we want the system which has less delay and also less static current flow. For that reason they find two standard level converters.

A. Dual Cascade Voltage Switching (DCVS)

This Dual cascade voltage switching is a standard type of level converter shown in Fig.2. which converts low volltage to high voltage by assigning vddl to non critical path of the circuit and vdd2 to critical path of the circuit.

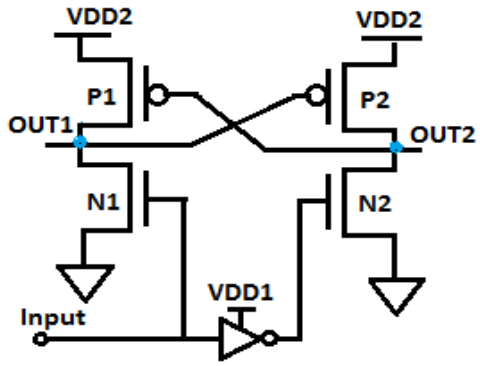

Fig.2.Dual Cascade Voltage Switching level converter.

This DCVS gates are operated at vdd1 and vdd2. By assigning like this will have a less impact to get a short circuit current flow from vdd to gnd as well as power consumption also reduces. In this approach we have cross coupled PMOS transistors p1, p2. This will supports as a load to the circuits. entire circuit acts like a differential pair. Means one side of P1 and N1 are pulled down. Other side will have pull up network be active. And transistors N1 and N2 regulates by the input signal. By using this approach which reduces static current (leakage) but it gradually increases dynamic power by the switching of the transistors and an inverter. After this will changes to 10 Transistor logic and 12 transistors logic. While increasing no. of level converters will have an increasing in power consumption.

B. Pass Transistors based Level Converter

In this pass transistors based level converter having four transistors and an inverter shown in Fig.3. Here we have a feedback based transistor named as M4. P type transistors M3 and M4 are assigning the VDD at 1v and the n type pass transistor M1 having the VDDL i.e. low voltage. These high and low voltages are assigning depending upon the critical path and the path density of the circuit. If the logic low is appears across the output of M3, it will be the input to the M4 feedback transistor. Then the M4 transistor is ON state and across the drain of M4 which gets logic high. This gets M3 be OFF and across the inverter we have logic high. Means it converts low logic to high logic level.

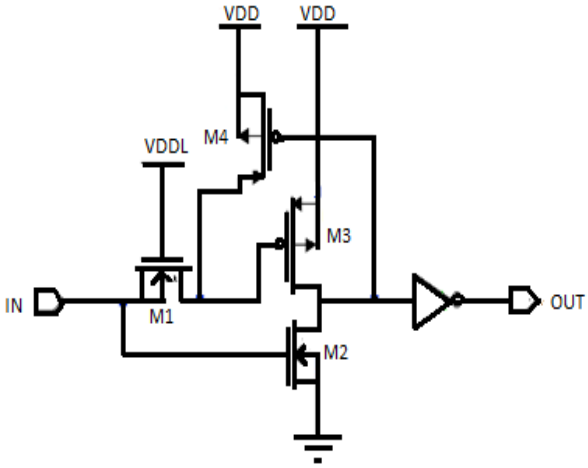

Fig.3. Pass Transistor level converter.

By using this approach we have major factors of delay and power which slightly decreases compared to standard level converter. But those are not appreciable. Delay factor have an impact on the number of transistors count and an inverter count. In the previous standard approach we have four transistors and an inverter. By using inverter we get very high delay to the system. And also we want to decrease power consumption of the device. For that reason we want to remove inverter this causes less delay to the system. We have different approaches like multi vth. This reduces delay as well as power consumption. In multi vth we have high vth transistors which reduce power consumption (leakage) and low vth transistors which reduce delay. But these level converters consists high number of transistors. Which has high complexity and also we want high switching capability. For that reason we proposed Multi vth feedback pass transistors level converter.

III. MULTI-THRESHOLD FEEDBACK PASS TRANSISTOR LEVEL CONVERTER (MTFP)

In this proposed approach is the combination of multi-threshold means high threshold transistors and low threshold transistors with a feedback transistor and all the transistors are the pass transistors shown in Fig. 4. By using the multi-threshold high threshold transistor reduces static power consumption and low threshold transistors reduces delay in the circuit. As well as the usage of pass transistors which will reduces transistors count.

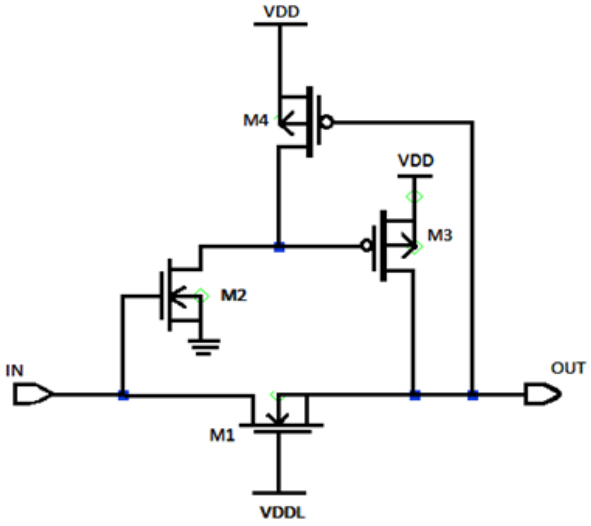

Fig.4. Multi-Threshold Feedback Pass transistor (MTFP).

In the above circuit M1, M2, M3, M4 are the four pass transistors. M1 & M2 are the low threshold NMOS pass transistors and M3 & M4 are the high threshold PMOS pass transistors. And M4 is the feedback transistor which makes a big impact to the circuit. Low voltage VDDL is given to the M1 NMOS pass transistor this makes transistor M1 is always ON mode. Means always the input passes through the output across this transistor. If the feedback transistor M4 is in OFF, then transistor M3 ON. And it passes high value across the output. Circuit operates as when we apply a low voltage i.e. VDDL to the input which ON transistor M2 because it is a Low threshold voltage NMOS pass transistor which Pass low

value across the drain of M2. Transistor M1 is always on because we apply VDDL to the input. Across M1 drain passes VDDL and it gives the input as feedback transistor M4. This condition makes M4 transistor OFF. Produces logic low to M3 this makes ON the M3. And produces output as logic High i.e. VDD. By using this approach we convert low logic to high logic with very less delay and less power consumption.

A. Level Converter Application of Low level to High level conversion in Multi-Supply Design

In order to verifying the level conversion of low level voltage to high level voltage conversion, we consider one SRAM memory device which stores one bit of information when we apply supply voltage of 1V. But we are assigning one level converter circuit in the place of input voltage of SRAM. We are applying low voltage VDDL to level converter it converts VDDL to high voltage i.e. 1V, then SRAM will operates. For low voltage VDDL we consider 2:1 multiplexer operating at a low voltage of 0.2V. Thus we consider 2:1 multiplexer at 0.2V and given to level converter. That level converter converts 0.2V to 1V and given to SRAM input. Hence, logic 1 to input of SRAM. It converts 0.2V to 1V by using our MTFP level converter which operates SRAM by using 0.2V. Shown in Fig.5.

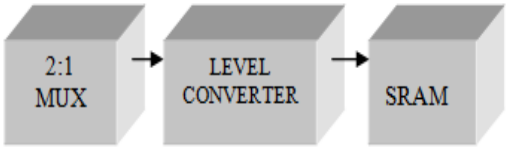

Fig.5.Low to High Level Conversion process application.

B. 2:1 Multiplexer Circuit

We consider 2:1 multiplexer with inputs as D1 and D2 with select inputs S and SB (inv of S) and output Z1. Shown in Fig.6.

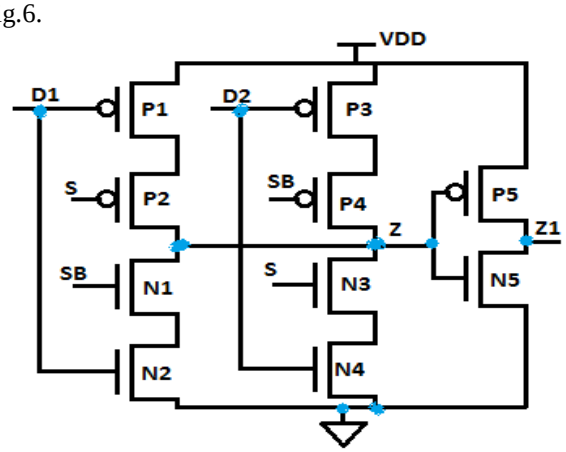

Fig.6. 2:1 Multiplexer[5].

Circuit operates as when select line S is in Logic low and SB is in logic high then output selects D1. Or else when select line S is in logic high and SB is in logic low then output selects D2. When the select line is logic low and SB having logic high then transistors N1 & P2 is in ON state. When D1 is at logic high then transistor N2 ON then Z is in logic low and output Z1 is in high it will passes supply voltage 0.2v across the output. Same as like select line is logic high and SB having logic low then transistors N3 & P4 is in ON state. When D2 is at logic high then transistor N4 ON then Z is in logic low and output Z1 is in high it will passes supply voltage 0.2v across the output. This 0.2V given to the input of MTFP level converter which converts 1V and apply to the supply voltage of SRAM.

C. SRAM Circuit

We consider 6 Transistor SRAM memory devices which operate at a voltage of 1V. Conventional CMOS 6T SRAM circuit consists of two access NMOS pass transistors AX1 and AX2. This will controls the read and write operational mode. And transistors P1,P2 and N1,N2 which forms cross coupled inverters. Means when P1 is ON then N2 be ON. This stores each bit in the memory cell when access transistor in saturation mode. shown in Fig.7

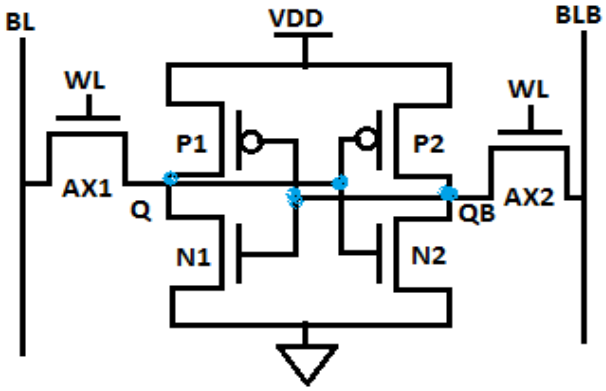

Fig.7. Conventional 6T SRAM[5].

Here circuit has two bit lines BL & BLB to store data in memory cell. And WL is for access data in write model. When Word line WL is logic high. Then output of our level converter is our SRAM Bit line BL. This value write in output Q. and BLB bit line value is written in QB. Means when WL is at logic high access transistors AX1, AX2 are ON, if BL is logic low then Q is logic low and QB is in logic high this turns transistors P2, N1 ON. When transistors AX1 & N1 ON, charge stored in BL goes to logic low. And AX2 & P2 are ON then charge stored in QB goes to high. When WL is in logic high and also BL at logic high, BLB at logic low then Q is at logic high and QB is logic low. This turns transistors P1 & N2 ON. When transistors AX1 & P1 are ON, charge stored at Q is logic high and transistors AX2 & N2 are ON, charge stored at QB is logic low.

BL=0: => QB stored 1V, Q stored 0V

BL=1: => Q stored 1V, Q stored 1V

We simulated first 2:1 multiplexer and then MTFP level converter and output of level converter converted to input of SRAM.

IV. SIMULATION RESULTS

We are designing schematic for Standard Level converter, pass transistor logic, 2:1 multiplexer, 6T SRAM and Multi-Threshold Feedback Pass Transistor level converter in Tanner EDA V15.0. For delay and power calculation we are using

32nm PTM model simulation in H-spice 2007. Compared delay and power calculation factors of standard, pass transistor and MTFP level converters.

TABLE I: Comparison of Power And Delay For All Approaches

INPUT VOLTAGE	Standard Level Converter		Pass Transistor Level Converter		MTFP Level Converter	
	Power (µW)	Delay (ps)	Power (µW)	Delay (ps)	Power (µW)	Delay (ps)
0.2V	5.8	242	3.8	160	3.4	120
0.3V	4.48	205	3.8	116	2.9	107
0.4V	4.02	113	2.52	82.4	2.05	70
0.5V	3.74	98.4	2.01	72.3	1.62	44.3
0.6V	3.02	82.2	1.82	62.6	1.47	32.48

TABLE II: Number of Transistors And Inverters Count

LEVEL CONVERTER MODEL	NO. OF TRANSISTORS	INVERTERS
STANDARD	4 transistor SVTH	1 INV
PASS Transistor	4 Transistors 2-HVTH, 2-LVTH	1 INV
MTFP	4 Transistors 2-HVTH, 2-LVTH	----

2:1 Multiplexer Output Waveform:

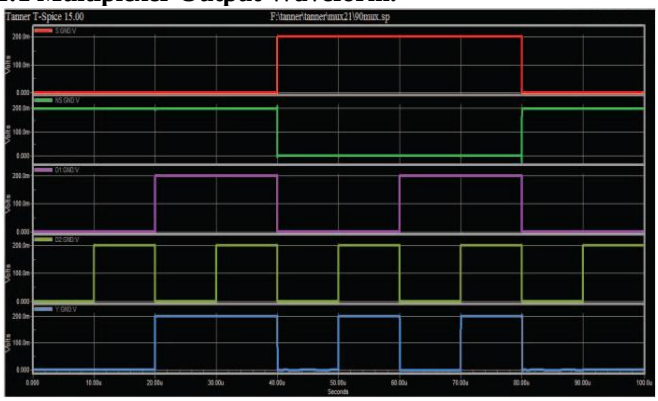

Fig.8. 2:1 Multiplexer output waveform.

6T SRAM Output Waveform:

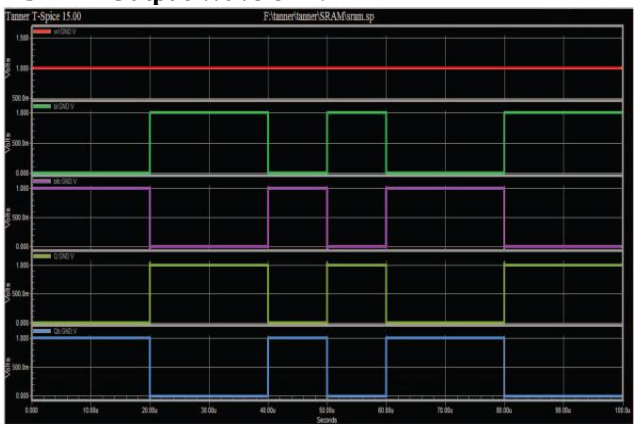

Fig. 9. Conventional 6T SRAM output waveform.

2:1 MUX to MTFP Level Converter To SRAM Waveform:

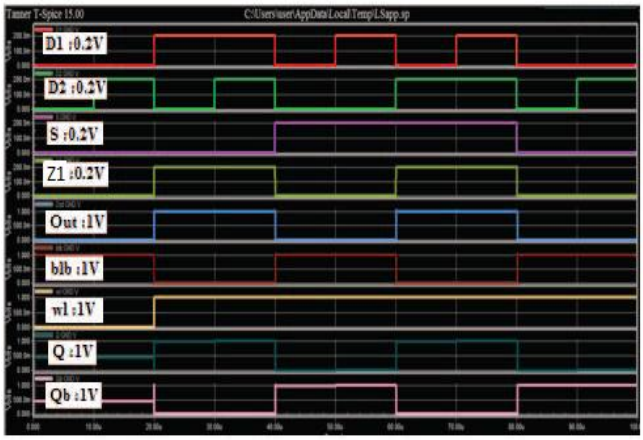

Fig. 10. MUX to MTFP and it to SRAM to get 1v ouput.

Comparison of power and delay for Standard level converter, pass transistor and MTFP level converters are shown in Table 1. And the transistors count and inverters count for all types of level converters shown in Table 2. in Fig.8 shows output schematic waveform of 2:1 multiplexer. Fig.9 shows output waveform of conventional 6T SRAM. Final output waveform says that for 2:1 multiplexer inputs D1 and D2 are operated at a voltage of 0.2V. And supply to the design is also 0.2V hence output is also 0.2V. Select line S, its output is Z1. And output of MTFP level converter is OUT. SRAM's WL & BLB as inputs and Q and QB are the outputs shown in Fig.10.

V. CONCLUSION

In this paper we present previous approaches of level converters with the proposed Multi-Threshold Feedback Pass Transistors (MTFP) level converter. This approach has multi threshold transistors for less power consumption and less delay and also pass transistors for decreasing the transistors count. From the above results proposed approach effectively reduces delay as well as power consumption of the system. And we also presented the application of low level voltage conversion to high level voltage conversion.

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