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Logical Effort Based Dual Mode Logic Gates

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Abstract: Logic optimization and timing estimations are basic tasks for digital circuit designers. Dual Mode Logic (DML) allows operation in two modes such as static and dynamic modes. DML gates can be switched between these two modes on feature very low power dissipation in the static mode and high speed of operation in dynamic mode which is achieved at the expense of increased power dissipation. We introduce the logical effort (LE) methodology for the CMOS-based family. The proposed methodology allows path length, delay and power optimization for number of stages with load. Logical effort is the transistor sizing optimization methodology reduces the delay and power with number of stages with any static logic gate. The proposed optimization is shown for dual mode logic gates with logical effort using Digital Schematic Tool (DSCH).

Keywords: Dual Mode Logic, Static Mode, Dynamic Mode, Logical Effort Methodology, Digital Schematic Tool (DSCH).

I. INTRODUCTION

LOGIC Optimization And Timing Estimations Are Basic Tasks For Digital Circuit Designers. The Logical Effort (LE) Method Was First Presented By Sutherland [1],[10] For Easy And Fast Evaluation And Optimization Of Delay In CMOS Logic Paths. Because Of Its Elegance, The LE Method Has Become A Very Popular Tool For Designing And Education Purposes And Is Adopted To Be The Basis For Several Computer-Aided-Design Tools. Although LE Is Mainly Used For Standard CMOS Logic, It Is Also Shown to Be Useful for Other Logic Families, Such As The Pass Transistor Logic [8].The Novel Dual Mode Logic (DML), Which Provides the designer with a very high level of switching between two modes of operation: 1) static and 2) dynamic modes. In the static mode, DML gates achieve very low power dissipation, with some degradation in performance, as compared with standard CMOS. On the other hand, dynamic operation of DML gates achieves very high speed at the expense of increased power dissipation. A basic DML gate is composed of any static logic family gate, which can be a conventional CMOS gate, and an additional transistor. DML gates have a very simple and intuitive structure, requiring n conventional sizing methodology to achieve the desired performance. Conventional LE methodology cannot be used with the DML family as it does not consider its unconventional sizing rules and topology.

The novel dual mode logic (DML) provides the designer with a very high level of flexibility. It allows on-the-fly switching between two modes of operation: 1) static and 2) dynamic modes. In the static mode, DML gates achieve very low power dissipation, with some degradation in performance, as compared with standard CMOS. On the other hand, dynamic operation of DML gates achieves very high speed at the expense of increased power dissipation. A basic DML gate is composed of any static logic family gate, which can be a conventional CMOS gate, and an additional transistor. DML gates have a very simple and intuitive structure, requiring n conventional sizing methodology to achieve the desired performance. Conventional LE methodology can't be used with the DML family as it does not consider its unconventional sizing rules and topology. The objective of this paper is to develop a simple method for minimizing delays and achieving an optimized number of stages in logical paths containing CMOS-based DML gates. A unified LE method is introduced for the delay evaluation and optimization of logic paths constructed with DML logic gates. DML-LE answers complete (UN approximate) design problems, which can be solved numerically, and simplifies these problems to a straightforward and easy computational problem [approximate and semi approximate (SA) solutions] with a unified analytic model. With this model, we can estimate the minimum to maximum error under delay approximation and the error in the target optimum number of stages for a given logic function. The efficiency of the developed method is shown by a comparison of the theoretical results, achieved using the proposed method with simulation results of Micro wind tool using a standard 32-nm technology

II.DML OVERVIEW

As previously mentioned [3], a basic DML gate architecture is composed of a static gate and an additional transistor M1, whose gate is connected to a global clock signal. In this paper, we specifically focus on DML gates [6] that utilize conventional CMOS gates for the static gate implementation. DML gates present two possible topologies: (1) Type A and (2) Type B, as shown in Fig1 accordingly. In the static mode of operation, the transistor M1 is turned off

by applying the high Clk signal for Type A and low Clk for TypeB topology. Therefore, the gates of both topologies operate in a similar way to the static logic gate, which here is a standard CMOS operation. To operate the gate in the dynamic mode, the Clk is Enabled, allowing for two separate phases: (1) pre charge (2) evaluation. During the pre charge phase, the output is charged to VDD in Type A gates and discharged to GND in Type B gates. During evaluation, the output is evaluated according to the values at the gate inputs.DML gates show a very robust operation in both static and dynamic modes under process variation at low supply voltages. The robustness in the dynamic mode is mainly achieved by the inherent active restorer (pull-up in Type A/pull-down in Type B) that also enabled glitch sustaining, charge leakage, and charge sharing. It is also shown that the proper sizing methodology is the key factor to achieve fast operation in the dynamic mode. Fig. 2 shows the sizing of CMOS-based DML gates that are optimized to a dynamic mode of operation, whereas Fig. 1(d) shows conventional sizing of a standard CMOS gate. The input and output capacitances of the DML gates are significantly reduced, as compared with CMOS gates, due to the utilization of minimal width transistors in the pull-up of Type 1 or pull-down in Type B networks.

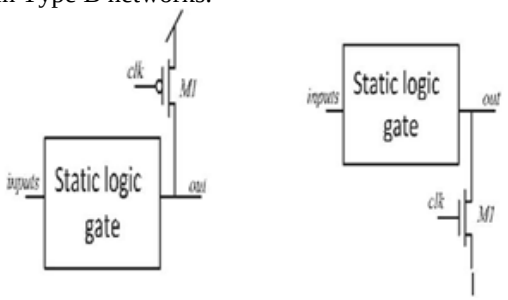

Fig1. DML Topology Type A, Type B.

The size of the pre charge transistor is kept equal S*W min to maintain a fast pre charge period despite the increase in the output load. Contrary to CMOS gates, each DML gate can be implemented in two ways, only one of which is efficient. The preferred topology is such that the pre charge transistor is placed in parallel to the stacked transistors, i.e., NOR in Type A is preferred over NAND, and NAND in Type B is preferred over NOR. In this case, the evaluation is performed the parallel transistors and therefore it is faster. As presented the optimal design methodology of DML gates is to serially connect Type A and TypeB gates, similarly to np-CMOS/NORA techniques. Even though this design allows maximum performance, area, minimization and improved power efficiency, serial connection of the same type gates is also possible. However, this case presents many drawbacks, such as the need of footer/header and severe glitching these well-explored problems are standard for dynamic gates design. DML strength is that static mode CMOS-based DML gates with transistor sizes optimized for the dynamic mode is actually a semi energy-optimal CMOS construction of a gate because of reduced static and switching energy consumption. The static operation of the DML gates is used to significantly reduce energy consumption at the expense of 2–4 times reduction in performance.

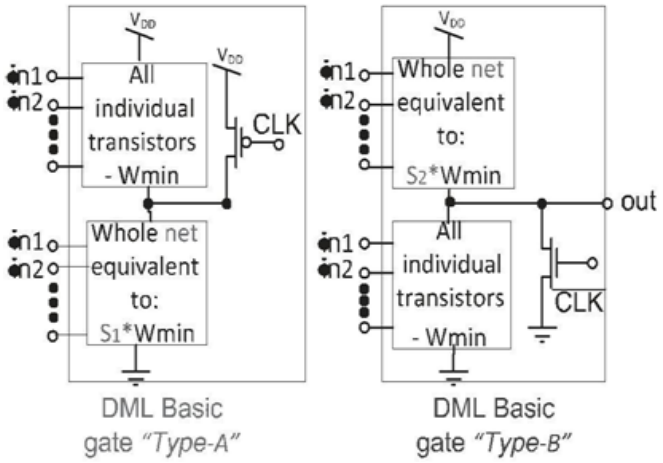

Fig2. CMOS-based DML gate with sizing factors.

A general approach is to optimize the delay for the dynamic mode of operation and operate the system in the static mode only in standby/low-energy mode without severe frequency restrictions that is magnitude of 2–4 times in performance is reasonable

III. LOGICAL EFFORT METHODOLOGY

Logical effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter delivering the same output current. Conventional methods use repetitive manual testing guided by Logical Effort (LE). To improve the performance of the DML gates, we will employ, modify, and approximate the well-explored LE technique Although LE is a well-known method and it is widely used by designers, there are few different metric and terminologies. LE is a simplified method of transistor sizing optimization to achieve an improved metrics of a combinational logic. The detailed description of conventional LE semantics is explained. These techniques are extended to include advance aspects of latest technologies such as temperature/voltage low voltage interconnect inclusion Energy - delay optimization and complex cells fitting According to this method, the gate normalized delay of stage i (Di) in a gates chain can be expressed as a sum of the stage (fi) and parasitic (pi) efforts as follows:

$$Di = fi + pi \quad (1)$$

Where

$$fi = gi \cdot hi \quad (2)$$

g_i is the LE of the stage; hi is the electrical effort

A. Logical effort CMOS inverter

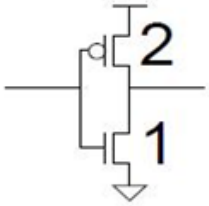

Fig3. CMOS Inverter.

The logical effort of CMOS inverter is to minimize the input capacitances of the gates of a path subject to maximum delay of the path. This problem can be articulated as sizing the gates of a logic path to minimize the sum of the path's gate input capacitances subject to the maximum delay of the path.

B. DML-LE Model for A Simple Inverter Chain

To optimize the performance of the DML gates, we will employ, modify, and approximate the well-explored LE technique [1], [2]. Although LE is a well-known method and it is widely used by designers, there are a few different metrics and terminologies. In Appendix I, the terminologies, which will be further used to develop the LE for CMOS-based DML gates, are presented. The LE formulation of DML is quite different from the conventional CMOS LE (and domino logic LE) [1.2], which is discussed in previous section. This is due to a unique structure and unconventional sizing methodology of DML gates. Achieving the optimal, non approximate solution is quite an exhausting task. Yet, by minor simplifications it can be solved rather similarly to the standard CMOS LE method. Here, first, a complete non approximated LE method for DML CMOS-based gates is presented. Although this solution is very precise, it is very complex and not designer friendly. Hence, two approximated solutions are presented. The complexity of these solutions is much lower, while achieving very high precision. Finally, a discussion about these approaches for DML LE for all CMOS-based gates is given.

C. Basic Assumptions:

DML gates are designed to optimize their dynamic mode delay and therefore only one transition among Tplh and Tphl, which is a part of the evaluation phase, should be considered. This means that only an equivalent resistance of the pull-down network (PDN) (nMOSs) will play a role in delay optimization of Type A gates and the pull-up network (PUN) (pMOSs) will be relevant in optimization of Type B gates. Although designing conventional CMOS gates the PUN is typically upsized with β, independently of the sizing factor effort, which is the sizing contribution of the load driving effort. This β is the outcome of the optimal delay of an unloaded gate. Typically, β, derived for an optimal gate delay, is different from βsym that achieves symmetric gate operation (Tphl = Tplh). However, in most technologies β is approximately equal to βsym (β ≈ βsym) [7]. With DML, each stand-alone gate would not be sized with β as the delay in the dynamic mode is determined by a single transition through PDN or PUN and therefore there is no need in symmetric transitions. Only one sizing factor, Si, for each i stage gate impacts the evaluation network and the precharge transistor, as shown in Fig. 1. In CMOS LE method, the normalization is performed to a standard CMOS inverter. DML gates are normalized to a standard minimal inverter (DML_INV) in Type A, which represents the minimal standalone gate delay unit. A minimal inverter of Type B presents an increased delay, as it evaluates the data through PMOS In this paper, we assume each DML chain would start with Type A gates followed by Type B gates (in a NORA/np-CMOS fashion [8], [9]). As mentioned in the previous section, γ is the fabrication technology-dependent factor that describes the transistor gate capacitance to transistor drain capacitance ratio. Typically, in most nanometer scale processes, γ is close to one. For CMOS inverters, it also describes the gate to drain capacitance of a single MOS transistor.

D. Defining the Problem for a Simple Inverter Chain

For obtaining the optimal sizing factors to a simple DML inverter chain, just assume a chain as shown in Fig. 2. The delay of a common gate i in the chain is known by (3). A normalized delay of every odd gate (Type A) and every even gate (Type B) can be shown in terms of the delay of minimal DML inverter tpo_DML as follows:

$$t_{pd\_i} = \underbrace{\frac{\ln(2).R_{min\_A}C_{D,min}}{\gamma'}}_{t_{p0\_DML}} \left(\overbrace{\frac{R_{gate}}{R_{inv}} \cdot \frac{C_{D,gate}}{C_{D,inv}}}^{p\_DML} \gamma' + \overbrace{\frac{R_{gate}}{R_{inv}} \cdot \frac{C_{G,gate}}{C_{G,inv}}}^{LE\_DML} \underbrace{\frac{C_{Load}}{C_{G,gate}}}_{f\_DML} \right) \quad (3)$$

Where $\mu_{n/p}$is defined as μ_n/μ_p, $S_i$is the ith stage sizing factor. Before, supposing an even number of inverters N in the chain, the delay of the chain can be stated by adding up the delays of all the chain constituents as follows

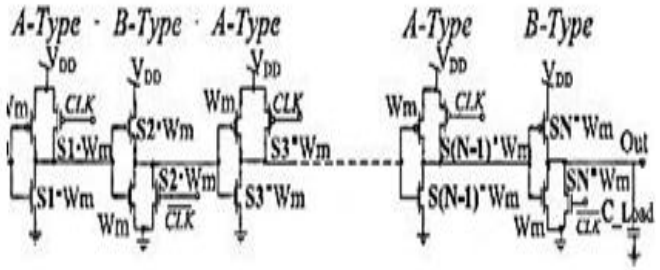

Fig4. DML Inverter chain.

$$D = \sum_i t_{pd\_i} = t_{p0\_DML} \times \left(\sum_{\substack{odd\_i \\ Type\_A}} \left(\frac{(2S_i+1)}{3S_i}\gamma' + \frac{S_{i+1}+1}{2S_i} \right) + \sum_{\substack{even\_i \\ Type\_A}} \left(\mu_{n/p} \left[\frac{(2S_i+1)}{3S_i}\gamma' + \frac{S_{i+1}+1}{2S_i} \right] \right) \right). \quad (4)$$

Where,
Si = width of the first stage of Type A ,Type B;
Si+1= width of the last stage of Type A, Type B;

In the following sections, three different solutions to the delay optimization problem are developed as follows: 1) complete Un approximated solution, 2) complete

approximated solution; and 3) partially/SA solution. These solutions are trading off complexity with accuracy.
Power=1.907 μw
Delay=0.073ns
Area :-
Dx=283 lambda (5.660 μm)
Dy=70 lambda (1.40 μm)
So, (Dx)(Dy)=19810 lambda^2 (7.924μm^2)
Power-Delay Product:-
PDP=(1.907 μW)(0.073 ns)= 0.139211 fW-s

D. Complete Un-approximated (CS) Method for the Sizing Factors of DML Inverter Chain

To solve this problem, differentiate (5) all Si factors of the chain and equate to zero, i.e., dD/dsi= 0. Afterwards simplifying and substituting γ, the resulting expression can be written for all odd i (6) and all even i (7):

$$\frac{S_i}{S_{i-1}} = \frac{(\gamma + 1 + S_{i+1})}{S_i} \frac{1}{\mu_{n/p}} \quad (5)$$

$$\frac{S_i}{S_{i-1}} = \frac{(\gamma + 1 + S_{i+1})}{S_i} \mu_{n/p} \quad (6)$$

Basically, the first gate in the chain could be all minimal sized transistors and so S1 = 1. Supposing, B = μn/p, B2 = (γ + 1) · μn/p (6) and (7) can be signified by the following set of expressions. This is a set of N equations with N indefinite variables; every equation is nonlinear, comprising mixed variable multiplication. In common, it can be solved numerically, as below:

$S_1 = 1$
$0 = B_2S_1 - S_{22} + BS_1S_3$
$0 = B_2S_2 - B_2S_{23} + BS_2S_4$
$0 = B_2S_3 - S_{24} + BS_3S_5$
$0 = B_2S_4 - B_2S_{25} + BS_4S_6$
...
...
...
...
...
$S_N^2 = B_2S_{N-1} + BS_{N-1} + BS_{N-1}S_{N+1}.$ (7)

This is the maximum optimal and accurate resolution for DML inverter chain sizing. But, solving it is a very exhausting task. This un-approximated solution (CS) is much more difficult than a simple CMOS LE optimal solution, which is resultant with no assumptions and approximations. DML CS method complexity is owing to a non-standard sizing of transistors, connected in parallel to the Clocked transistor. Succeeding suppositions will be used in the rest of this project. Leading, as solved in previous section, the first gate of any examined chain will be least sized, i.e., S_1=1. S_1can be indiscriminate to some possible sizes in accordance with any input capacitance. Another, even number of stages N is presumed. This is due to the topology of DML chains that mainly consists of Type B gates succeeding Type Agates. Still, the solution for the chain, which has an odd number of stages, can be easily consequential using the same methodology.
Load effect on CS:
Power=64.720 μw

Area:
Dx=534 lambda (8.010 μm)
Dy=476 lambda (7.140 μm)
So, (Dx)(Dy)=254184 lambda (57.194μm^2)

Power-Delay Product: For CS,

PDP_{CS}=(64.720 μW)(0.073 ns)= 4.72456 fW-s

E. Complete Approximated (CA) Method for the Sizing Factors of DML Inverter Chain

To decrease the difficulty of the LE method, a CA solution, which trades off the accuracy and complexity, is derived. It is beforehand conferred that (5) defines a common delay expression for the whole chain, supposing an even number of inverters N. The CA method assumes that the involvement of minimal transistors to the drain and gate capacitances is negligible in contrast with 2Si and with Si+1, for every stage of the chain. As exposed in Section V, ignoring these transistors, for complex gates increases the accuracy w.r.t inverters. Then, (5) can be expressed by

$$D = \sum_N D_i = t_{p0\_DML}\left(\sum_{\substack{odd\_i \\ Type\_A}}\left(\frac{(2S_i+1)}{3S_i}\gamma' + \frac{S_{i+1}+1}{2S_i}\right) + \sum_{\substack{even\_i \\ Type\_B}}\left(\mu_{n/p}\left[\frac{(2S_i+1)}{3S_i}\gamma' + \frac{S_{i+1}+1}{2S_i}\right]\right)\right). \quad (8)$$

It is beforehand conferred that (5) defines a common delay expression for the whole chain, supposing an even number of inverters N. The CA method assumes that the involvement of minimal transistors to the drain and gate capacitances is negligible in contrast with 2Si and with Si+1, for every stage of the chain. As exposed in Section V, ignoring these transistors, for complex gates increases the accuracy w.r.t inverters. Then, (5) can be expressed by

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These suppositions are acceptable only when the output load capacitance of the chain is high. The sizing factors Si is affected by the large load capacitance. As soon as S_i increases, along the chain; this calculation will increase in accuracy for high i values. After generalization, (9) can be revised as follows:

$$D = \sum_{N} D_i = t_{p0\_DML} \times \left(\sum_{\substack{odd\_i \\ Type\_A}} \left(\frac{2}{3}\gamma' + \frac{S_{i+1}}{2S_i} \right) + \sum_{\substack{even\_i \\ Type\_B}} \left(\mu_{n/p} \left[\frac{2}{3}\gamma' + \frac{S_{i+1}}{2S_i} \right] \right) \right) \quad (10)$$

Table1

S_1	S_2	S_3	S_4	S_5	S_N	S_{N+1}
1	$\sqrt{\mu_{n/p}}A^{0.5}$	A	$\sqrt{\mu_{n/p}}A^{1.5}$	A^2	$\sqrt{\mu_{n/p}}A^{(\frac{N}{2}-0.5)}$	$A^{\frac{N}{2}}$

Inverter Chain Sizing Factors Si of the CA Method

The sizing factors solution for this CA method is quite related to standard CMOS solution. Likewise to CMOS, the upsizing factor is constant. But every even stage is factored by an additional $\sqrt{\mu_{n/p}}$. On behalf of the N-size chain, the sizing factors can be shown in series as in table I where A is expressed in (14). In CMOS, the sizing factors are resulted from the load to input capacitance ratio, while in DML, they are illustrated by the ratio of the first to last sizing factors.

$$\text{In CMOS: } F = \frac{C_{\text{Load}}}{C_{\text{in},g}} = f^N, f = \sqrt[N]{F}. \quad (11)$$

$$\text{In DML: } \frac{S_{N+1}}{S_1} = A^{\frac{N}{2}},\ F_{\text{DML}} = \frac{S_{N+1}}{S_1} = f_{\text{DML}}{}^{\frac{N}{2}} \quad (12)$$

$$A = f_{\text{DML}} = \sqrt[N]{F_{\text{DML}}} \quad (14)$$

where assuming $S_1 = 1$, S_{N+1} can be extracted from

$$\frac{(S_{N+1}+1)\,WL_{\min}}{(S_1+1)\,WL_{\min}} = \frac{S_{N+1}+1}{2} = \frac{C_{\text{Load}}}{C_{\text{in},g}}. \quad (15)$$

The delay of the total chain is denoted by the sum of delays of all n logic stages and of all the added n inverters. Distinguishing the chain delay by N then equating to zero as follows

$$\underbrace{\gamma\left(\mu_{n/p}{}^{-0.5} + \mu_{n/p}{}^{0.5}\right)}_{C_1} + \sqrt[N]{F_{\text{DML}}} - \frac{\sqrt[N]{F_{\text{DML}}} * \ln(F_{\text{DML}})}{N} = 0 \quad (16)$$

Delay for Load Capacitance effect in CA Method:

Load effection CA: Power=19.067µw
Area :
Dx=505lambda (7.575 µm)
Dy=441 lambda (6.615 µm)
So,(Dx)(Dy)=222705lambda (50.11µm^2)

Power-Delay Product:-
For CA,
PDP_{CA}=(19.067 µW)(0.146 ns)= 2.783782 fW-s

F. SA Method for the Sizing Factors of DML Inverter Chain

To compromise between the CS and CA methods, a SA approach is introduced. The SA approach is comparatively high precision with compact computational effort w.r.t the CS method. It is done by ignoring only the first and the second terms of (5), as compared with neglecting all terms of the gate and drain capacitances (Complete Approximated method).The solution of the SA is very easy and in addition to the ordinary CMOS LE optimization manual design, the designer should utilize a simple lookup table (given in above).
Load effect on SA:
Power=39.180 µw

Area :
Dx=550 lambda (8.25 µm) Dy=493 lambda (7.395 µm)

So, (Dx)(Dy)=271150 lambda (61.01µm^2)

Power-Delay Product:
For SA,
PDP_{SA}=(39.180 µW)(0.146 ns)= 6.61249 fW-s

F. Comparison of the DML Methods

Now, a comparison between the SA, CS, and CA techniques is shown. The techniques are compared with simplicity, accuracy and depend on delay in the optimum no of stages

Table2

DML Methods	Power(µw)	Area(µm^2)	Power Delay Product (fW-s)
CA	19.067	50.11	2.7837
CS	64.720	57.194	4.72456
SA	39.180	61.01	6.61249

IV. RESULT ANALYSIS

The proposed Logical effort technique with the Dual mode logic gates all circuits have been simulated in a DSCH technology .The DML inverter chain was sized based on CMOS technology and scaled to get minimum power and delay.

STAGE 1: It describes about the design of complex network scheme by using logical effort methodology.

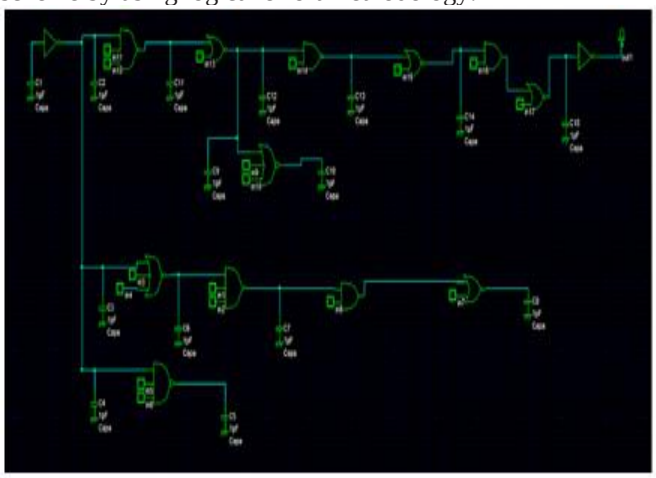

Fig5. Circuit Design.

STAGE 2: we are generating the Verilog file by using digital schematic tool.

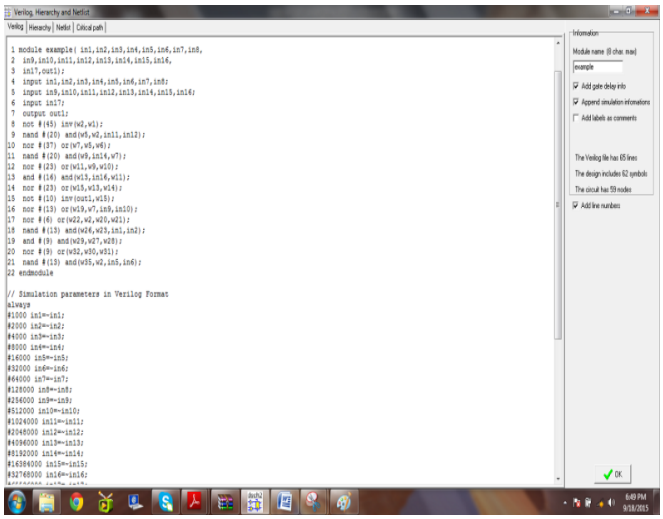

Fig6. Verilog File Generation.

STAGE 3: Layout Design

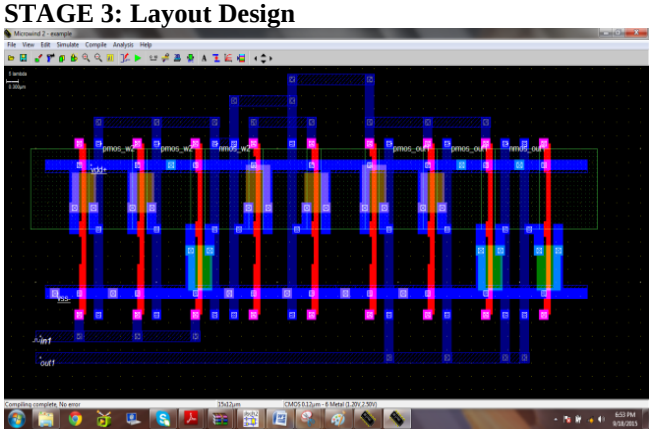

Fig7. Layout Design.

STAGE 4: By varying the transistor sizes i.e. pull up and pull down ratio we are getting different power values which are listed below in table3.

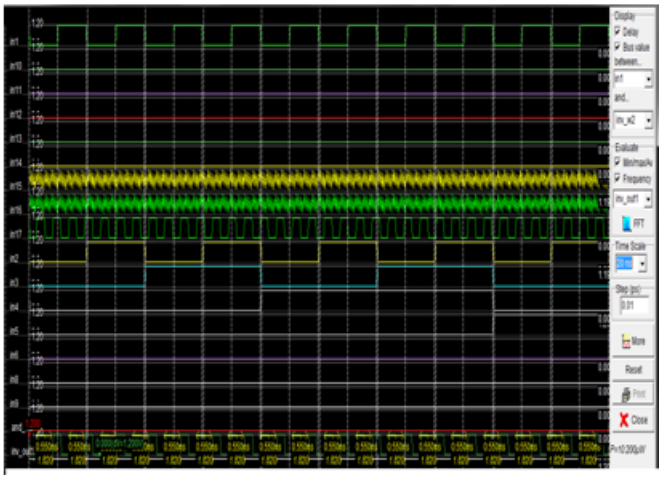

Fig8. Simulation Results.

Table3

WIDTH (µm)	DELAY (Ps)	POWER(µw)
2/1	28	25.743
1.5/0.75	24.64	21.88
1/0.5	20.93	19.178
0.75/0.375	18.55	16.629
0.5/0.25	15.83	13.866

V. CONCLUSION

A novel LE approach for CMOS-based DML logic networks was presented. The proposed approach allowed an efficient optimization of DML logic networks for maximum performance in the dynamic mode of operation, which was the focus of this paper. DML logic, optimized according to the proposed LE methods, allowed extended flexibility in optimizing various structures of DML networks. This optimization utilized the DML inherent properties of significantly reduced parasitic capacitance and ultralow power dissipation in the static operation mode. This paper presented three different approaches, which traded off between computation complexity and accuracy. The complex CS method was only addressed for error analysis of the other methods. The CA method was identical to CMOS LE computation with very small error and the SA method was also identical to the CMOS LE computation aiding one more lookup table (which easily derived for all cases and loads). We showed that with these tools only a design can achieve very high performance results. Simulation results, carried out in a DSCH TOOL process, proved the efficiency of the proposed approach and compared it with existing CMOS LE.

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