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Power Efficient FFT Architecture using SMSS for High Speed Real Time Application

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Abstract: This paper consist of an implementation of shared multiplier scheduling scheme on radix-2 FFT architecture for High speed real time application. It is an area efficient architecture. In these days many application require concurrent computation of multiple independent FFT and their outputs are in normal order. So this paper introduces sixteen point pipelined FFT processor using shared multiplier scheduling scheme for computation of two independent data stream. Here N/2 point DIT FFT and N/2 point DIF FFT is to process odd and even samples of 2 data streams individually. This SMSS technique reduces total number of complex multiplier and hardware complexity. The proposed pipelined FFT processor based on SMSS is designed using Modelsim and implemented in XILINX ISE TOOL and coded by Verilog HDL language.

Keywords: DIT and DIF, MIMO, Multipath Delay Commutator, Odd and Even Samples, Radix 2 Pipelined FFT, SMSS, Xilinx ISE Tool.

I. INTRODUCTION

FFT Processor plays an important role in OFDM techniques, image processing and signal processing application. Such application requires high speed FFT Processor to meet demands for higher data rates. For implementing such processors several architectures are used. They are Memory based, Reconfigurable and Pipelined FFT. Memory based FFT processor [1], [2] are used to achieve small area. Here it use Application specific instruction set processor to meet flexibility for FFT computation. Reconfigurable FFT processors [3] are used to select various FFT sizes on processor so it will reduce hardware complexity. The pipelined processors [4] are used for achieving high throughput rate. Pipelined architectures are classified into single path delay commutator (SDC), single path feedback (SPF), Multi path delay feedback (MDF) and multipath delay commutator (MDC). This technique is based on MDC. MDC architectures produce high throughput rate and simple synchronizing control using multi data path. In MDC Radix size is high then throughput is high. The FFT architectures in [5]–[8], performance multiple independent data streams. In which all the data streams are processed by a single FFT processor in [5] and [8]. In [5], four independent data streams are processed one by one. In [5] eight data streams are processed at two domains. But in these two processor, multiple data outputs are not obtained in parallel. In [3], one to four input streams are treated using multiple data paths for wireless local area network application. The architectures in [5]–[7] do not have any specific bit reversal circuit. The modified architecture is 16 point pipelined FFT Processor based on shared multiplier scheduling scheme. In FFT computation several multiplications are required. These multiplications are performed by SMSS technique. In the existing structure, the P_2 and Q_2 stages consist of several complex multiplication during 8 point DIT and DIF operation. So this stage will increase the hardware complexity. So by using SMSS Technique, it will reduce the area, power and delay of existing structure.

II. EXISTING FFT ARCHITECTURE

In this the structure is designed to process two individual data streams continuously with less amount of hardware. The odd inputs, which are in normal order, are first bit reversed and then they are processed by N/2-point DITFFT. The even samples are directly processed by N/2-point DIF FFT, then their output are in bit reversed order. Therefore, the outputs of DIF FFT are bit reversed. The outputs of the 2- N/2 FFTs are further processed by the two-parallel butterflies to generate N-point FFT in normal order. Here bit reversing is executed by the scheduling registers, they are delaying the samples. So, FFT structure not need any circuit to bit reverse the data. As a result, this structure need less number of registers than the previous FFT designs. The structure consist of two 8 point Multipath Delay Commutator FFT architectures for executing 2 data streams. The data streams are separated into odd and even samples by delay commutator unit at the left side of SW_1.Inputs are received by shift registers in the delay commutator unit and it will bit reverse the odd input and the registers are called reordering shift registers or RSRs. The RSR in the last stage bit reverse the partially processed even data. Then the two BF_2 in the last stage produce N point FFT outputs in normal order.

In the P_3 and Q_3 stage, two data stream from SW_2 are added together, because of this, these lines are represented by thick lines. The existing architecture in Fig. 1 is dissociate into six stages P_1, P_2, P_3, Q_1, Q_2, and Q_3.The Reordering shift registers can be reorder the odd input data in the P_1 and Q_1stage and reorder the partially processed even data in the last stage P_3 and Q_3. Eight point DIT and DIF operations are executed in P_2 and Q_2 stages. The inputs from P_1 and Q_1 can be forwarded to P_2 andQ_2 or vice versa through $SW_1$and the data from P_2 and Q_2 can be forwarded to P_3 and Q_3, or vice versa through switch SW_2. The switches SW_1 and SW_2 are used for swap the input path and propagate the input to different levels. In the normal mode, the switches transfer the data from P_1, P_2, P_3, and P_4 to Q_1, Q_2, Q_3, and Q_4. In the swap mode, the switches transfer the data from P_1, P_2, P_3, and P_4 to Q_3, Q_4, Q_1, and Q_2, respectively. During first N/2 clock cycles SW_1 is in swap mode and it is in the normal mode during N/2 + 1 to N and during first N/2 clock cycles SW_2 is in the normal mode and it is in the swap mode during N/2 + 1 to N. Here SW_1 and SW_2 are operating in different mode at any time and change their mode during every N/2 clock cycle.

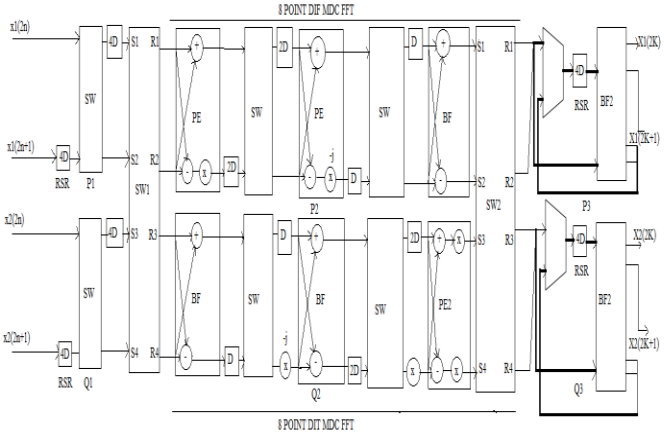

Fig 1. Existing FFT architecture.

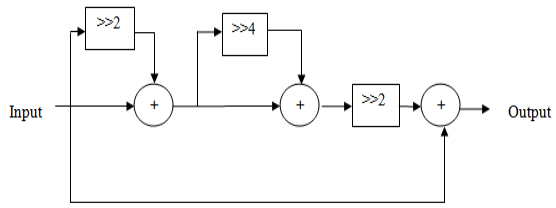

Fig 2. Circuit diagram of the bit-parallel multiplication by 1/ $\sqrt{2}$.

III. ARCHITECTURE OF SMSS BASED FFT

The proposed SMSS based 16 point pipelined FFT processor based on MDC architecture produce high throughput and low hardware complexity. In the existing processor, the P_2 and Q_2 stages consist of several complex multiplication during 8 point DIT and DIF operation. So this stage will increase the hardware complexity. In existing architecture, the multiplication coefficient used in P_2 and Q_2 stages is 0.707,-1 and 1. In PE_2 both multiplication coefficients are 0.707.So in this stage a SMSS technique is introduced. In the existing processor the multiplication by 0.707 can employ a bit parallel multiplier according to the equation (1), and the circuit diagram is shown in figure 2.

$$\text{Output} = \text{in} * \sqrt{2}/2 = \text{in} * [1 + (1+2^{-2})(2^{-6}-2^{-2})] \text{ ---- (1)}$$

The resulting circuit uses three additions and three barrel shift operations. The SMSS Architecture is shown in figure 3. This method is designed based on Mux working. It consists of delay elements that will Store the required multiplication coefficients.

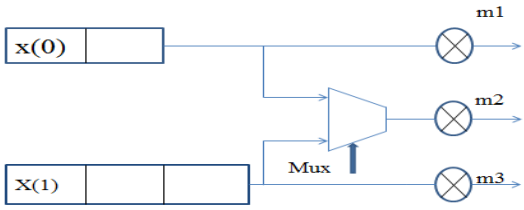

Fig 3. SMSS Architecture.

In proposed method, The SMSS technique is applied in PE_2 stage of Existing processor. Because both adder and subtractor output is multiplied by 0.707 multiplication coefficient. So the adder and subtractor output of PE2 stage is selected by using shared multiplier scheduling scheme. Then it is multiplied by 0.707 and the output is stored in a register. Therefore by using this technique we can reduce the area, power and time delay of architecture compared to existing processor. The modified FFT architecture is shown in figure 4.

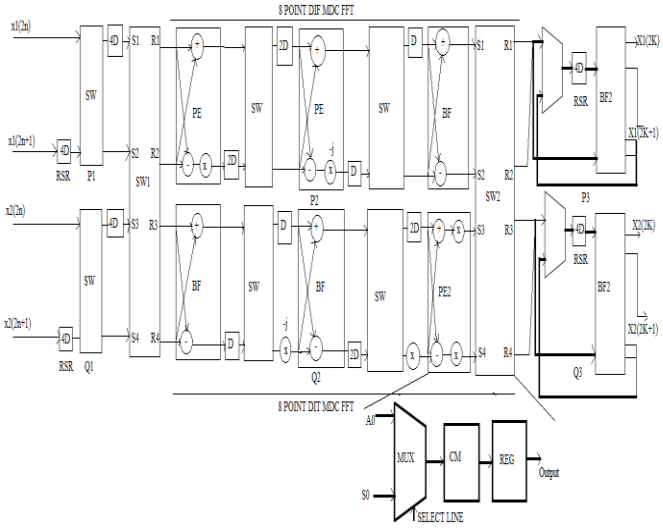

Fig 4. SMSS Based FFT architecture.

IV. RESULT AND DISCUSSION

Fig 5 shows the output waveform of SMSS based 16 point FFT architecture. In which four inputs and four outputs are presented and it is simulated in Modelsim tool. It is implemented in Xilinx ISE 14.4 tool. RTL Schematic of FFT architecture is shown in figure 6 and comparison of the proposed FFT architecture with prior FFT Architecture is shown in table 1.

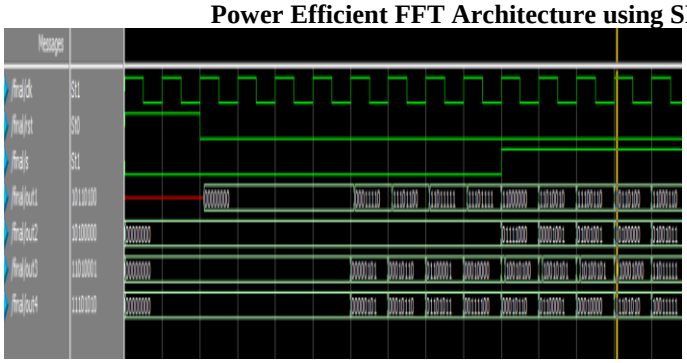

Fig 5.16 point SMSS Based FFT Waveform.

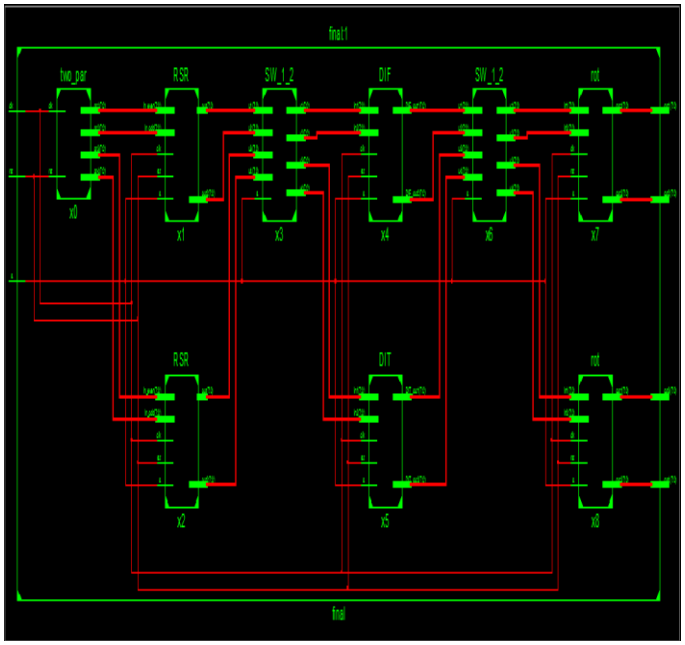

Fig 6. RTL Schematic of 16-point SMSS based FFT Architecture.

Table 1. Comparison of the proposed FFT architecture with prior FFT Architecture

Comparison	Proposed Method	Existing Method
Junction Temperature(C)	32.5	29.3
Power(W)	0.166	0.287
Delay(ns)	12.834	18.672

By adopting this technique, it can reduce the power and delay of the existing Work. Power consumption of the modified 16 point pipelined FFT architecture is about 0.166W at 1000 MHz and delay of the architectures are 12.834ns. From the comparison between existing and modified FFT architecture, we know that the SMSS technique reduce the Power, delay, junction of the architecture.

V. CONCLUSION

Here a technique to reduce the area of pipelined FFT architecture is presented. This technique reduce number of complex multiplication and hardware complexity. Here this structure produce outputs are in normal order. The modified processor can execute two individual input streams continuously, thus it will perfect for many high speed wireless communication applications.

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