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Design And Implementation of Efficient Flip-Flops using Transmission Gate Logic

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Abstract: The field of digital VLSI is looking towards the low power and high speed digital systems. The use of VLSI in high performance computing has been rising at a fast rate. This paper enumerates design of Single Edge Triggered (SET) Flip-Flop, Double Edge Triggered (DET) Flip-Flop, True Single Phase Clock (TSPC) Flip-Flop, Clocked CMOS(C2CMOS) Flip-Flop and Push Pull Isolation D Flip-Flops(PPI-DFF) using transmission gate logic. Push Pull Isolation D flip-flop proves to be fastest and more efficient among all others. These flip flops are used in various applications such as microprocessors, digital systems, registers. These flip-flops have small area and low power consumption and are implemented in Tanner EDA. These flip flops are measured with respect to Area (µm), Transistor Count (no. of PMOS and NMOS), Propagation Delay (ns), Power Delay Product (PDP) and Power Consumption.

Keywords: Flip-FLOP Topologies, Transmission Gate Logic, Propagation Delay (NS), Power Consumption, Power Delay Product (PDP) and Transistor Count.

I. INTRODUCTION

A Flip-flop is a bi-stable circuit which is used to store data in the form of either '1' or '0'. D flip-flop is most frequently used because of its simplicity. In present scenario there is an ever interesting demand for fast and robust devices. This paper provides respective contributions:

- Different flip flop topologies and their corresponding outputs.
- Comparison of different topologies in terms of various parameters.
- Finally, it concludes with the best D-flip flop circuit.

II. DIFFERENT TYPES OF D FLIP-FLOP TOPOLOGIES

This section contains different types of D flip-flop topologies such as Single Edge Triggered (SET) Flip-Flop, Double Edge Triggered (DET) Flip-Flop, True Single Phase Clock (TSPC) Flip-Flop, Clocked CMOS (C2CMOS) Flip-Flop, Push Pull Isolation D Flip-Flops (PPI-DFF).

A. Single Edge Triggered (Set) D- Flip Flop

The below Fig.1 can be constructed with the help of ten transistors. In this, we have two phases master and slave. The master is functional when the clock goes high i.e. C='1'.The output is stored at the node X .The slave consists of a feedback loop and the outputs Y and Q. The slave is activated when clock is low i.e. C='0'and produces output at Y and Q. Logic level is maintained even if the clock is grounded. In this data value '0' is given to the circuit then it passes through the inverter and gives the value of '1' i.e., in master stage. Whereas in slave, when clock is set to '1' it passes the value through NMOS transistor and gives required value at the inverter i.e., output(Y). When this passes through the inverter it gives inverter value of the output(Y). It consists of less number of transistors when compared to all other flip-flops. Above schematic is designed with the help of tanner EDA.

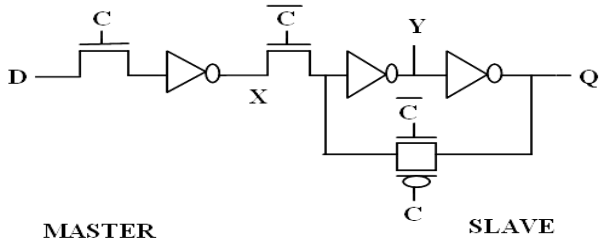

Fig.1. Ten-transistor (10T) SET D-Flip-Flop.

B. Double Edge Triggered (DET) Flip Flop

The below Fig.2 is based on both positive and negative edge triggering and it is shown in below Figure.

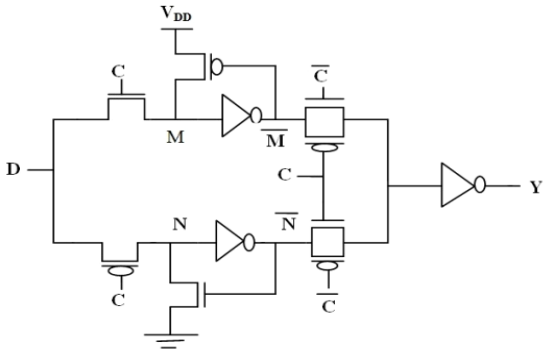

Fig.2. Fourteen Transistors (14T) DET D-Flip Flop.

It consists of two states i.e., master and slave. It also consists of two data phases i.e., higher and the bottom phases. The

higher data phase is of NMOS pass transistor, which is active only when clock is high (C='1'). The bottom data phase is of PMOS pass transistor, which is active only when the applied clock is low (C='0'). Both these have feedback (FB) loops. Higher feedback (FB) loop is of an inverter and PMOS while the bottom feedback (FB) path is of an inverter and NMOS. The pass transistor present in the higher feedback (FB) phase acts as pull up transistor and pulls the value of node M to VDD. This is present in the bottom feedback (FB) phase acts as pull down transistor and pulls the value of node N to GND. When logic high is given as input the value at node M becomes logic high with help of PMOS transistor. When the clock i.e., C='0' the transmission gate present at the higher data phase is active and it transmits the corresponding value present at the node Mbar to the output Y by inverting the value, similarly when clock (C) ='1' the transmission gate at lower data path is active and the data at node Y is transmitted to output (Y) with help of inverter.Figure 2 is the schematic of this flip-flop is designed with help of Tanner EDA tool.

C. True Single Phase Clock

The below Fig.3 can be constructed with the help of sixteen transistors.

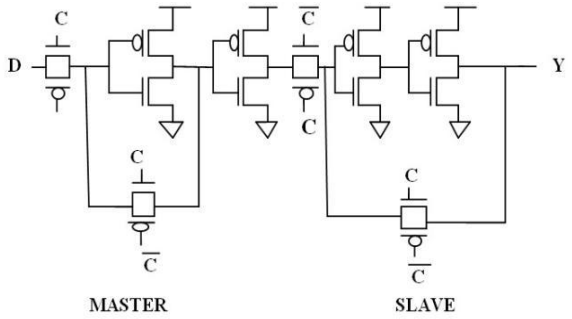

Fig.3. Sixteen- Transistors (16T) TSPC.

The architectures of above figure can be drawn. It also has two stages master and slave. When C='1' the transmission gate at the master stage is active and the input given at D is present at the output (Y) of the master stage, the input (D) passes through two inverter so the output is same as the input (D). The master stage has a feedback loop which consists of a transmission gate which is used to store the output of master so that it can be given as input to the slave when it is activated. The slave is activated when C='0'.When the slave is activate is master is OFF and does not take any input. Each phase (master and slave) produces the output same as input i.e. True value, in single phase so it is known as True single phase clock. This schematic is designed by using i.e., Tanner EDA tool.

D. Clocked CMOS (C2CMOS) D-Flip Flop

The below Fig.4 can be constructed using twenty transistors. It consists of twenty transistors and it is of two phases i.e., master and slave. When the data input (D) is given to the circuit then it passes PMOS and NMOS transistors and then it will obtain a value. Then it passes through the inverter and gives the corresponding value at the master phase. Hence it is connected to feedback (FB) path and it obtains the same value at this phase. Whereas in slave it is active when clock(C) is set to '0' and it also consists of inverter and passes the corresponding value at the output(Y). The schematic of Clocked CMOS is designed with the help of Tanner EDA.

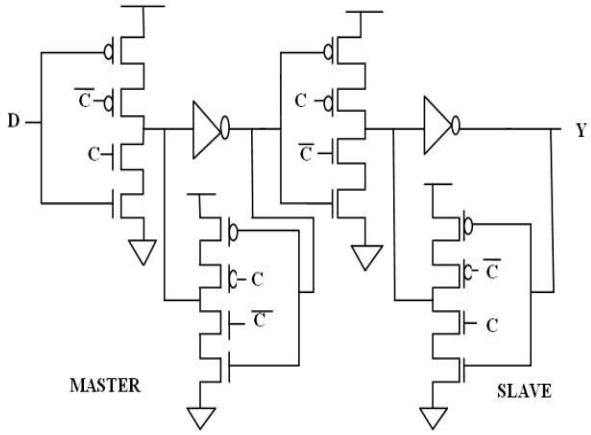

Fig.4. Twenty-Transistor (20T) Clocked CMOS.

E. Push Pull Isolation D Flip-Flop (PPI-DFF)

"Push Pull Isolation D Flip-Flop (PPI-DFF)" consists of an additional PMOSFETs in order to isolate feedback path and was comparatively more robust than the others as evident fro1m the simulation results. The Push Pull Isolation D Flip-Flop is as shown in below Fig.5.

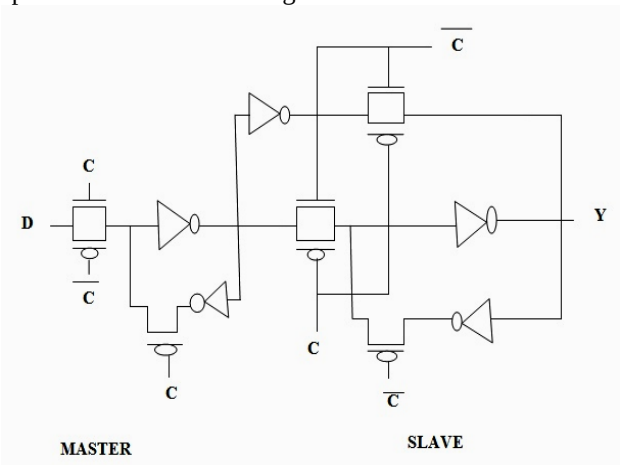

Fig.5. Push Pull Isolation D Flip-Flop (PPI-DFF).

In push pull isolation when C='1' the master stage is active and the input D reaches the output of master whose value is invert of the applied input (D). The two stages of Push Pull Isolation has a feedback in which a PMOS and an inverter are connected in series, this connection isolates the feedback. When C='0' the slave is activated and the output of the slave is invert of the applied input(D) , the slave takes the output of master as input(D).While 'C' is low the feedback in master will be ON and when 'C' is high the feedback in slave will be ON and master will be OFF.

III. SIMULATION RESULTS

Simulation results of this paper is as shown in bellow Figs. 6 to 15.

A. Schematic Of Set

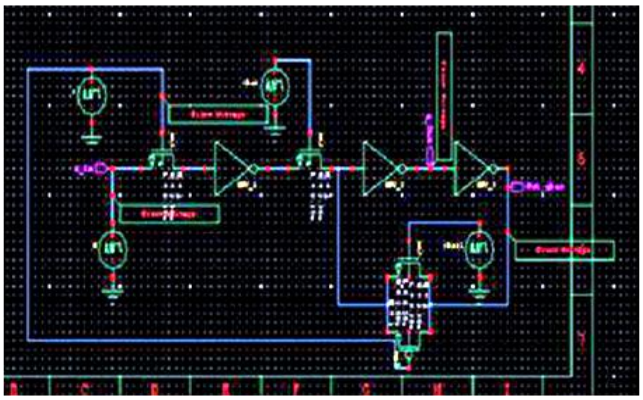

Fig.6. Schematic of SET.

B. Output Waveforms Of Set

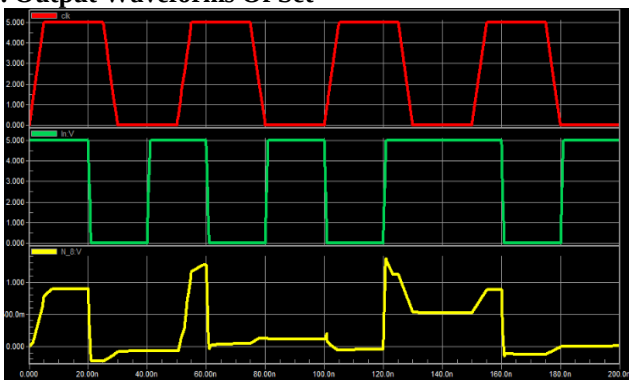

Fig.7. Output Waveform of SET.

C. Schematic Of Det

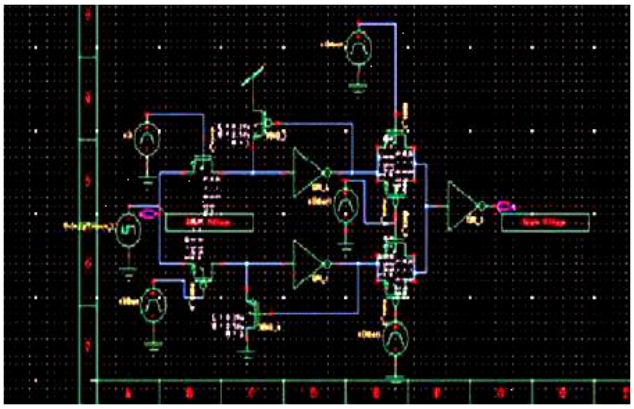

Fig.8.Schematic of DET.

D. Output Waveforms Of Det

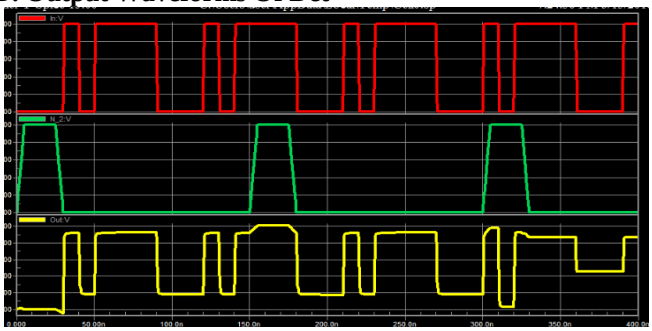

Fig.9. Output Waveform of DET.

E. Schematic Of TSPC

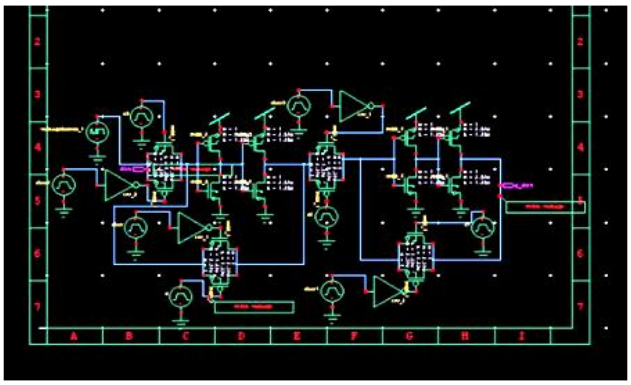

Fig.10. Schematic of TSPC.

F. Output Waveforms Of TSPC

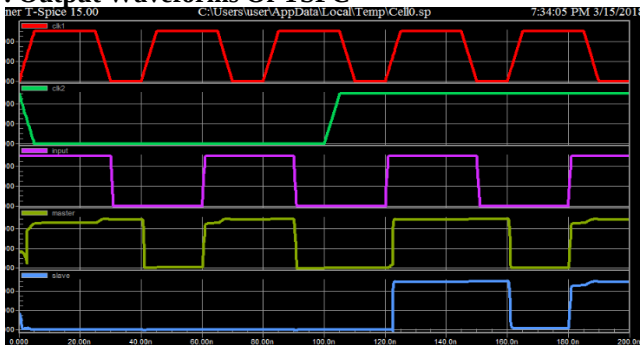

Fig.11. Output Waveform of TSPC.

G. Schematic Of Clocked CMOS

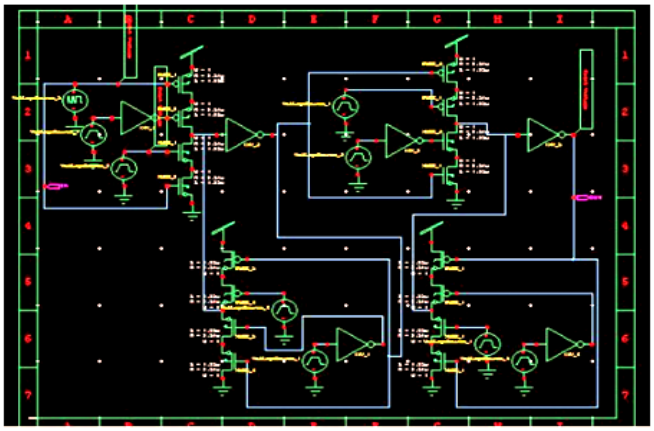

Fig.12. Schematic of Clocked CMOS.

H. Output Waveform Of Clocked CMOS

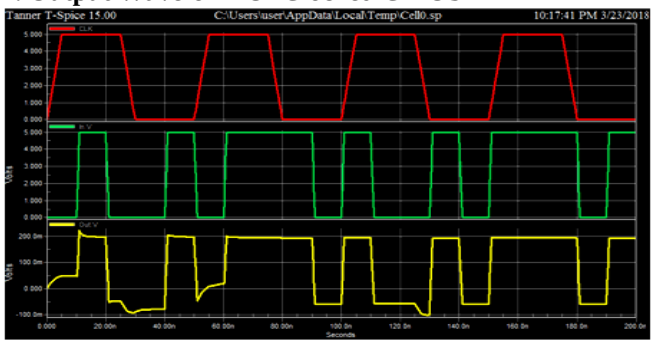

Fig.13. Output Waveform of Clocked CMOS.

I. Schematic Of Push Pull Isolation Flip-Flop (PPI-DFF)

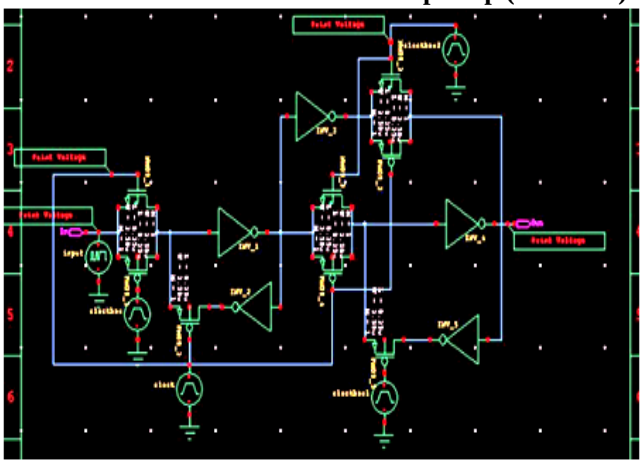

Fig.14. Schematic of Push Pull Isolation Flip-Flop.

J. Output Waveforms Of Push Pull Isolation D Flip-Flop (PPI-DFF)

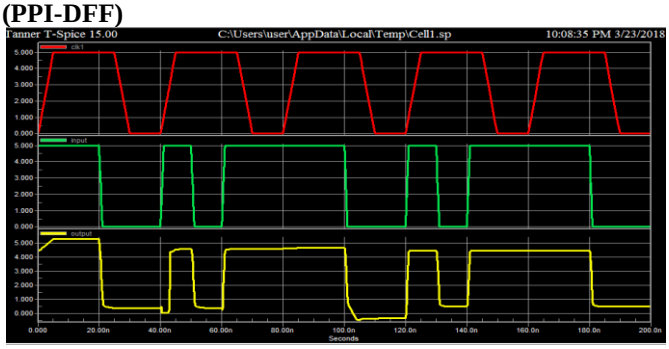

Fig.15. Output Waveform of Push Pull Isolation D FlipFlop.

TABLE I: Performance Comparision of D Flip-Flops

Various D Flip Flops	PARAMETERS				
	Transistor Count	Area (μm^2)	Power (mw)	Delay(s)	Power Delay Product (pJ)
SET	10	6.25	1.07	1.2	1.2
DET	14	8.75	0.5	1.5	0.75
TSPC	16	10	1.1	1.01	1.11
C2CMOS	20	12.5	0.3	0.88	0.26
Push Pull Isolation	18	11.25	0.5	1.07	0.53

V. CONCLUSION

The comparison of flip-flops has been performed with area, delay and power dissipation and transistor count. With respect to area and number of transistor count SET and DET are better because of its simple circuitry while with respect to power dissipation C2CMOS and Push pull isolation flip-flop shows better result. Considerate the suitability of flip-flops and selecting the best topology for a given application is an important issue; the low power design SET is suitable for portable applications. Hence we conclude that by the above comparisons it proved that the C2CMOS and Push pull isolation D Flip-Flop (PPI-DFF) shows better results when compared with SET, DET and TSPC, this means that both architectures are suitable in low power, fast switching applications. In future, these flip flops can be implemented in small area with low power consumption.

VI. REFERENCE

[1] Uming Ko, and Balsara P.T., "High performance energy-efficient D-flip-flop circuits," IEEE Transactions on Very Large Scale Integration Systems.

[2]Himanshu Kumar, Amresh Kumar, Aminul Islam "Comparative Analysis of D Flip-Flops in Terms of Delay and its Variability", IEEE 2015.

[3] Yu Chien-Cheng, Chin Ping-Yuan, (2005) "Design of Low-Power Double-Edge Triggered Flip-Flop", 6th international IEEE Conference on ASIC 0-7803-9210-8/05/IEEE.

[4] A. Islam, M. Hasan, T. Iqbal, M. A. Kafeel, "Variability Analysis of MTJ-based Circuit," IEEE 3rd International Conference on Computer and communication Technology.

[5] K.G.Sharma, Tripti Sharma, B.P.Singh, Manisha Sharma, "Modified SET D-Flip Flop Design for Low-Power VLSI Applications",978-1-4244-9190-2/11/ IEEE 2011.

[6] Pooja Joshi, Saurabh Khandelwal, Shyam Akashe, "Implementation of Low Power Flip Flops Design in Nanometer Regime", IEEE 2015 Fifth International Conference on Advanced Computing & Communication Technologies.