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MAC Unit Design using Multiplier & Ripple Carry Adder

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Abstract: Digital signal processing is the application of mathematical operations to digitally represented signals. DSP processors share basic features designed to support high-performance, repetitive, numerically intensive tasks. MAC is the most important block in DSP system. High throughput multiplier accumulator (MAC) is always a key element to achieve a high-performance digital signal processing application for real time signal processing applications. This is because speed and throughput rate are always the concerns of digital signal processing systems. This is because, the limited battery energy of these portable products restricts the power consumption of the system. The goal of this project is to design the VLSI implementation of MAC for high-speed DSP applications. For designing the MAC, various multipliers and adders are considered. The total operation is coded with VHDL, synthesized and simulated using Xillinx ISE 6.2i.

Keywords: VHDL, Multipliers, Adders.

I. INTRODUCTION

As integrated circuit technology has improved to allow more and more components on a chip, digital systems have continued to grow in complexity. As digital systems have become more complex, detailed design of the systems at the gate and flip-flop level has become very tedious and time consuming. For this reason, use of hardware description languages in the digital design process continues to grow in importance. A hardware description language allows a digital system to be designed and debugged at a higher level before conversion to the gate and flip-flop level. DSP processors are microprocessorsdesigned to perform digital signal processing the mathematical manipulation of digitally represented signals. Digital signal processing is one of the core technologies in rapidly growing application areas such as wireless communications, audio and video processing, and industrial control. Digital signal processing (DSP) applications constitute the critical operations which usually involve many multiplications and accumulations. Hence, high throughput multiplier accumulator (MAC) is always a key element to achieve a high-performance digital signal processing application for real time signal processing applications. In the last few years, the main consideration of MAC design has been to enhance its speed. This is because speed and throughput rate are always the concerns of digital signal processing systems. Due to the increase of portable electronic products, low power designs have also become major considerations. This is because the limited battery energy of these portable products restricts the power consumption of the system. Therefore, the motivation behind this project is to investigate various pipelined MAC architectures and circuit and the design techniques which are suitable for the implementation of high throughput signal processing algorithms. The goal of this project is to design the VLSI implementation of pipelined MAC for high-speed DSP applications. For designing the MAC, various architectures of multipliers and adders are considered. The total process is coded with Verilog to describe the hardware.

II. OVERVIEW OF MAC UNIT

Multiply-accumulate operation is one of the basic arithmetic operations extensively used in modern digital signal processing(DSP). The MAC unit provides high-speed multiplication, multiplication with cumulative addition, multiplication with cumulative subtraction, saturation, and clear-to-zero functions. Therefore, the main motivation is to investigate various pipelined MAC architectures and circuit and the design techniques which are suitable for the implementation of high through put signal processing algorithms. Hence, a high-speed MAC that is capable of supporting multiple precisions and parallel operations is highly desirable. MAC is composed of an adder, multiplier and an accumulator. The implementation of the multiplier is in the form of Booth Multiplier. The adder used is Ripple Carry Adder. The layout of this adder is simple which allows for fast design time. The Parallel in Parallel out (PIPO) shift register is used as the accumulator. The inputs for the MAC are to be fetched from memory location and fed to the multiplier block of the MAC, which will perform multiplication and give the result to the adder which will accumulate the result and then will store the result into a memory location. This entire process is to be achieved in a single clock cycle in the architecture of the MAC unit. The MAC design consists of one 8-bit booth multiplier, one 16-bit ripple carry adder & a 17-bit accumulator using PIPO shift register.

To multiply the values of A and B, Booth Multiplier is used instead of conventional multiplier because this is simple to design. However to gain better performance, parallel multipliers are used as they are the fastest but the designs are much more complex. Hence, when regularity, high performance & low power are primary concerns, Booth Multipliers tend to be the primary choice. Apparently, together with the utilization of Booth multiplier approach, ripple carry adder as the adder and PIPO shift register as the accumulator, this MAC design can enhance the MAC unit speed so as to gain better system performance. The product of Xi x Yi is always fed back into the 17-bit accumulator and then added again with the next product Xi x Yi. This MAC unit is capable of multiplying and adding with previous product consecutively. Hence, output =Σ Xi Yi. The design of 8x8 multiplier unit is carried out that can perform accumulation on 17 bit number. This MAC unit has 17 bit output and its operation is to add repeatedly the multiplication results. The total design area can be inspected by observing the total count of transistors. Several other parameters can be calculated as well. Fig.1 shows the basic block diagram of the MAC unit. The equation for MAC operation can be given as:

$$a = a + (bxc) \quad (1)$$

where a is an accumulator register,
b is the multiplier & c is the multiplicand.

Eq(1) depicts the basic operation of the MAC unit. Fig.2 depicts the block diagram of MAC unit consisting of Booth multiplier, Ripple carry adder & PIPO shift register.

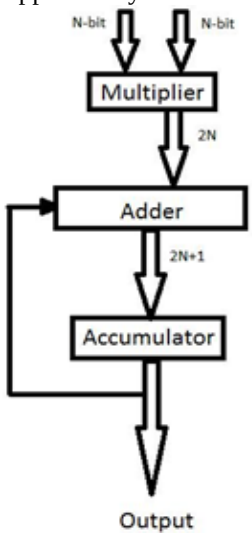

Fig.1. Basic MAC unit.

III. OPERATION

Basically a MAC unit employs a fast multiplier fitted in the data path and the multiplied output of multiplier is fed into a fast adder which is set to zero initially. The result of addition is stored in an accumulator register. The MAC unit should be able to produce output in one clock cycle and the new result of addition is added to the previous one and stored in the accumulator register. A single MAC unit has multiplier, adder, and accumulator. The most typical feature that differentiates a DSP from any General Purpose Processor is the Multiply and Accumulate unit. All DSP Algorithms would require some form of the Multiplication and Accumulation Operation. This is the most important block in DSP systems. It is composed of an adder, multiplier and the accumulator. Usually adders implemented in DSPs are Ripple Carry Adders, Carry-Select or Carry-Save adders, as speed is of utmost importance in a DSP. Basically the multiplier will multiply the inputs and give the results to the adder, which will add the multiplier results to the previously accumulated results. This operation eases the computation of the most important formula i.e. b(n)x(n-k) which is needed in filters, Fourier analyzers, etc. The inputs for the MAC are supposed to be fetched from some memory location and fed to the multiplier block of the MAC, which will perform multiplication and give the result to adder which will accumulate the result and then if needed will also store the result into a memory location. This entire process is to be achieved in a single clock cycle. The MAC operation can be verified with the help of the simulation waveform.

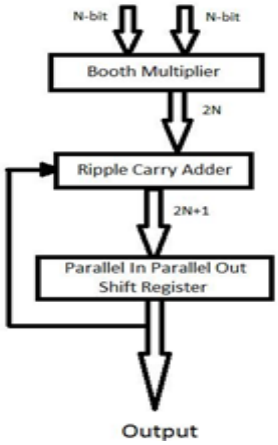

Fig. 2. Block diagram of MAC unit.

IV. EXPERIMENTAL RESULTS

The Verilog code of MAC process is synthesized and simulated using Xilinx ISE 6.2i. It is implemented on xc3s1000-5fg456 FPGA device. Table 1 shows the estimated values of the logic utilization of the devices used. Hence, the estimated values of the numerous logic utilized in the design of the MAC unit can be calculated i.e. % utilization of no. of LUTs, slices, input/output blocks, global clock etc. Fig.3 shows the RTL schematic of MAC Operation. It has two input ports and two output ports.

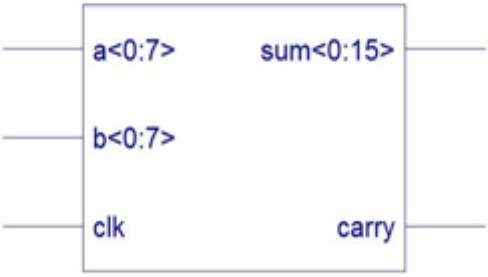

Fig.3. RTL view of MAC operation.

TABLE I: Device Utilization Summary (Estimated Values)

Logic Utilization	Used	Available	Utilization
Number of Slices	172	7680	2%
Number of Slice flip flops	17	15360	0%
Number of 4 input LUTs	313	15360	2%
Number of bonded IOBs	33	333	9%
Number of GCLKs	1	8	12%

Fig.4 displays the simulation waveform of MAC operation.

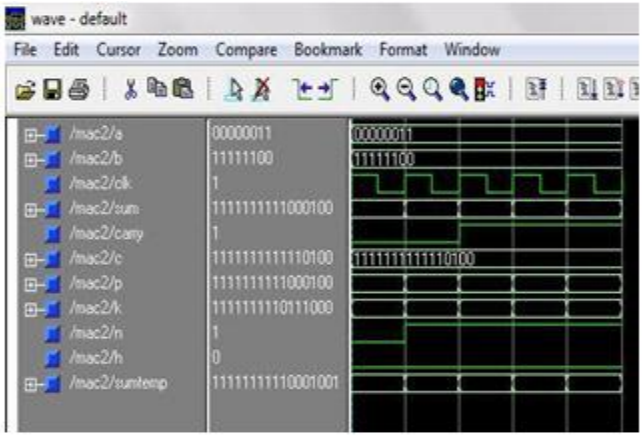

Fig.4. Simulation waveform of MAC operation.

V. CONCLUSION

The MAC process is coded with verilog and synthesized using Xilinx ISE 6.2i. The MAC process is implemented using xc3s1000-5fg456 FPGA Xilinx device. The synthesis results of the MAC unit have been calculated as can be seen in Table 2. Here, same FPGA device (part number & speed grade) with the same design constraints implied for the synthesis of the MAC unit has been targeted. This MAC unit is generally preferred for simpler designs. The experimental test shows that the results have been validated. Table 2 shows the synthesis results of the Multiply Accumulate Unit.

TABLE II: Synthesis Results of MAC Unit

FPGA Device Package	Xc3s1000-5fg456
Minimum period	4.5 ns
Maximum frequency	MHz

VI. REFERENCES

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